<table>
<tr><th colspan="6">Department of Electronics and Telecommunication Engineering</th></tr>
<tr><td>Name</td><td colspan="4">KULKARNI PRASAD ANANT</td><td>  </td></tr>
<tr><td>Date of Birth</td><td colspan="5">26/02/1976</td></tr>
<tr><td rowspan="2">Education Qualifications</td><td>UG</td><td colspan="2">PG</td><td colspan="2">PhD</td></tr>
<tr><td>BE (Electronics Engineering)</td><td colspan="2">ME (Electrical with Control System)</td><td colspan="2">Electronics Engineering (Area :VLSI Design)</td></tr>
<tr><td rowspan="2">Work Experience</td><td>Teaching</td><td>Research</td><td>Industry</td><td colspan="2">Others</td></tr>
<tr><td>26</td><td>-</td><td>3</td><td colspan="2">-</td></tr>
<tr><td>Area of Specialization</td><td colspan="5">VLSI</td></tr>
<tr><td>Courses taught</td><td colspan="5">Digital Circuit design , Microcontrollers , VLSI, Control system , Electrical</td></tr>
<tr><td rowspan="3">Research guidance (Number of Students)</td><td>Under Graduate projects</td><td colspan="4">7</td></tr>
<tr><td>Masters</td><td colspan="4">-</td></tr>
<tr><td>Ph.D (Completed / Thesis Submitted / Ongoing)</td><td colspan="4">-</td></tr>
<tr><td>External Fund Received</td><td colspan="5">-</td></tr>
<tr><td>Patent (Filed / published / Granted) details</td><td colspan="5">▪ Design and Implement FFT processor with High Throughput and Optimum Area with Reduced Complexity.
▪ Copyright: “ASIC Design of Radix-2,8-Point FFT Processor”, Extract from Register of Copyrights, Government of India, Registration Number L-99658/2021.
▪ Copyright: “Home TechCare using IoT”, Extract from Register of Copyrights, Government of India, Registration Number L-113546/2022.
▪ Copyright: “SELF DRIVING CAR”, Extract from Register of Copyrights,</td></tr>
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	Government of India, Registration Number L-1343529/2023. ▪ **Copyright:** "Digital VLSI Lab Manual", Extract from Register of Copyrights, Government of India, Registration Number L-139764/2023 ▪ **Patent Published:** "ASIC Design of Radix-2,8-Point FFT Processor," Indian Patent Office, Government of India, Application Number 202121004749, Mar.2021.		
No. of papers published in National/International Journals/Conferences	**4**	**8**	
Research Publications (No. of papers in National/International Journals / Conferences and No. of Books/ Book Chapters published	**Scopus/SCI indexed journals: 02** **Peer reviewed / UGC journals: 02** **IEEE/Springer conferences: 08** **Books/Book Chapters: -** **Other International Conferences: -** **National Conference: 04**		
Projects Carried out	1. **Object Detection using FPGA** (project in collaboration with IISER Mohali 2. **Tool Condition Monitoring: (On going 2022)** Project work is based on machine learning to classify the state of the finished product processed on the lathe machine by sensing the temperature, vibration and position of the table. 3. **Interfacing of wireless protocols to FPGA and controlling devices (2017)** 4. **UDP: Simulation of Asynchronous Transfer Mode Computer Network. (2004-2005)** The user defined protocol with header having 53 cell. This protocol having 5-byte header and 48-byte payload. Scrambling facility is also available for payload. 5. **Multi-Channel Ethernet** with **Oasis PVT Ltd (2001) as** apart PG Diploma.		
Other major responsibilities	**NBA Co-Ordinator , APMS Portal Co-ordinator ,Institute level Publicity Team, FDP convenor ,IETE-ISF convener .**		