# **Agnel Charities**

# Fr. C. Rodrigues Institute of Technology

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An Autonomous Institute Affiliated to the University of Mumbai



# Handbook Containing Rules, Regulations, Curriculum & Examination Schemes for

Honours / Minor / Honours in Research Degree Programs in B. Tech

Approved By: Academic Council of Fr.C.Rodrigues Institute of Technology

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### A. Abbreviations

HMCC	Honours or Minor Core Course
HML	Honours or Minor Laboratory
HMMP	Honours or Minor Mini Project
RP	Research Project
RPC	Research Project Coursework

#### Introduction

In the AICTE's Approval Process Handbook-2020-21, there's a strong emphasis on incorporating Elective Courses in Emerging Areas across all branches of Engineering and Technology. Consequently, the University of Mumbai launched Honours and Minor Degree Programs in Engineering during the Academic Year 2022-23.

Agnel Charities' Fr.C. Rodrigues Institute of Technology (FCRIT) has chosen to continue offering these Honours and Minor degrees autonomously, recognizing their potential to equip students with specialized knowledge or research in emerging fields of interest. This initiative is geared towards enhancing students' proficiency in these areas and empowering them with valuable skills.

RHM 2401.1 Proposed Honours, Minor, and Honours in Research Degree Programs at

#### FCRIT

Students shall have the flexibility to pursue one of three designations: (i) B. Tech with an Honours Degree, (ii) B. Tech with a Minor Degree, or (iii) B. Tech with Honours in Research Degree.

Students who fulfil the eligibility criteria outlined RHM 2401.3 of this handbook have the option to pursue an additional 18 credits from the fifth to eighth semesters. This enables them to attain a B. Tech degree with either Honours, Minor, or Honours in Research designation.

For the B. Tech Degree in Honours, students are required to choose additional courses within a similar technology discipline.

For the B. Tech Degree in Minor, students are required to choose additional courses in a different technology discipline.

For B. Tech Degree in Honours with Research, students need to engage in a research project, either from reputable research organizations like IIT, TIFR, etc. or in exceptional cases at FCRIT depending upon available infrastructure and domain expertize of the guide, in the similar technology discipline.

#### • Proposed Honours and Minor Degree specializations

- a) Artificial Intelligence & Machine Learning
- b) Blockchain
- c) Augmented Reality/Virtual Reality
- d) Data Science
- e) Cyber Security
- f) IoT & Embedded Systems
- g) Network Security
- h) Data Analytics & AI
- i) Additive Manufacturing
- j) Supply Chain
- k) Aeronautical Engineering

2

- l) VLSI
- m) Electric Vehicle
- n) Renewable Energy
- o) Power Electronics and Drives

RHM 2401.2

Mapping as 'Honours' or 'Minor' Degree Program with Existing B. Tech Programs Please refer to Table RHM 2401.2.1 for the mapping of a particular specialization either as an Honours or as a Minor degree with existing B. Tech programs.

Table RHM 2401.2.1: Mapping as 'Honours' or 'Minor' Degree Program with Existing B. TechPrograms

Honours/Minor Specialization	B. Tech Programs that can offer this as an Honours Degree	B. Tech Programs that can offerthis as a Minor Degree
Artificial Intelligence & Machine Learning Blockchain Augmented Reality/Virtual Reality Data Science Cyber Security IoT & Embedded Systems Network Security	<ol> <li>Computer Engineering</li> <li>Electronics &amp; Telecommunication Engineering</li> <li>Information Technology</li> </ol>	<ol> <li>Mechanical Engineering</li> <li>Electrical Engineering</li> </ol>
Data Analytics and AIAdditive ManufacturingSupply ChainAeronautical Engineering	Mechanical Engineering	<ol> <li>Computer Engineering</li> <li>Electronics &amp; Telecommunication Engineering</li> <li>Electrical Engineering</li> <li>Information Technology</li> </ol>
VLSI	Electronics & Telecommunication Engineering	<ol> <li>Computer Engineering</li> <li>Mechanical Engineering</li> <li>Electrical Engineering</li> <li>Information Technology</li> </ol>
Electric Vehicle	<ol> <li>Electrical Engineering</li> <li>Mechanical Engineering</li> </ol>	<ol> <li>Computer Engineering</li> <li>Electronics &amp; Telecommunication Engineering</li> <li>Information Technology</li> </ol>

RHM 2401.3 Eligibility Criteria for Honours, Minor, and Honours in Research DegreePrograms for Students

- a) At the end of semester IV students shall not have any live backlog for any of the courses in semesters I to IV.
- b) Students must achieve a CGPI of 7.5 or higher based on semesters I to IV results.
- c) Direct Second Year (DSE) admitted students shall not have any live backlog at the end of semester IV for any of the courses in semesters III to IV and must achieve a CGPI of 7.5 or higher based on semesters III and IV results.
- d) Each eligible student may choose to pursue either one Honours or one Minor or Honours in Research Program and accordingly shall do course registration

3

from semester V to VIII.

- e) Participation in Honours/Minor/Honours in Research Degree programs is voluntary.
- f) Honours/Minor/Honours in Research degree programs are only available during regular engineering studies.
- g) Completion of the Honours/Minor/Honours in Research degree program must be accomplished within four semesters as stipulated.

# RHM 2401.4 Honours/Minor Degree Programs Scheme and Structure

Credit courses for Honours, Minor, and Honours in Research programs will be available from Semester V through Semester VIII. The curriculum structure and examination scheme for B. Tech with Honours and Minor are detailed in Table RHM 2401.4.1 and RHM 2401.4.2, respectively. For the Honours/Minor/Honours in Research specializedcourses grades will be awarded. However, the marks will not be included in CGPI calculations.

#### Table RHM 2401.4.1: Curriculum Structure for Honours/Minor Degree Program

Course Type	Sem	Course Code	Course Name	ourse Name (Contact Hours)		C	Credits	Assig	ned	
				L	Р	Т	L	Р	Т	Total
НМСС	V	HMCCXX501	Honours/Minor Core Course-I	3			3			3
HMCC	VI	HMCCXX602	Honours/Minor Core Course –II	3			3			3
HMCC	VII	HMCCXX703	Honours/Minor Core Course -III	4			4			4
HML	VII	HMLXX701	Honours/Minor Laboratory-I		4			2		2
HMCC	VIII	HMCCXX804	Honours/Minor Core Course -IV	4			4			4
HMMP	VIII	HMMPXX801	Honours/Minor Mini Project		6			2		2
	Tota						14	04		18

	,	Table RHM 240	1.4.2: Examination \$	Scheme for Hor	ours/Min	or Degre	ee Program	1	
					Exa	mination	Scheme		
Course Type	Sem	Course Code	Course Name	Assessment S		End Sem Exam	Exar Duratio Theo (in H	on for ory	Total
				Continuous Assessment	Mid Sem Exam	(ESE)	Mid Sem	End Sem	
НМСС	v	HMCCXX501	Honours/Minor Core Course-I	20	30	50	1.5	2	100
HMCC	VI	HMCCXX602	Honours/Minor Core Course -II	20	30	50	1.5	2	100
HMCC	VII	HMCCXX703	Honours/Minor Core Course -III	20	30	50	1.5	2	100
HML	VII	HMLXX701	Honours/Minor Lab-I	50					50
НМСС	VIII	HMCCXX804	Honours/Minor Core Course -IV	20	30	50	1.5	2	100
HMMP	VIII	HMMPXX801	Honours/Minor Mini Project	50		50			100
	•		Total	180	120	250			550

RHM 2401.5 Course Details for the Honours/Minor Degree Programs

Table RHM2401.5.1 gives course details for the Honours/Minor Degree Programs specializations offered by EXTC Department

Table RHM 2401.5.1: Course Details for Honours/Minors Degree Programs offered by EXTC Department

Honours/	Semester V	Semester VI	Semes	ster VII	Semest	er VIII
Minor Degree Programs	Theory Course	Theory Course	Theory Course	Lab Course	Theory Course	Mini Project
	HMC-I	HMC-II	HMC-III	HML-I	HMC-IV	HMMP
	HMCAL501	HMCAL602	HMCAL703	HMLAL701	HMCAL804	HMMPAL801
Artificial Intelligence & Machine Learning	Knowledge Engineering	Foundation of Machine Learning	Deep Learning	Artificial Intelligence & Machine Learning Laboratory	Advanced AI	Mini Project
	HMCIE501	HMCIE602	HMCIE703	HMLIE701	HMCIE804	HMMPIE801
IoT & Embedded Systems	Sensors & IoT Protocols	Embedded System Design with RTOS	Dynamic paradigms of IoT	IoTES Laboratory	AIoT & Industry 5.0	Mini Project
	HMCNS501	HMCNS602	HMCNS703	HMLNS701	HMCNS804	HMMPNS801
Network Security	Introduction to Communication Networks	Computer Networks & Security	Encryption Algorithms for Networks	NS Laboratory	Advanced Topics in Network Security	Mini Project
VLSI	HMCVL501	HMCVL602	HMCVL703	HMLVL701	HMCVL804	HMMPVL801
	CMOS VLSI	System Architecture	ASIC Design	VLSI Laboratory	System on Chip Design	Mini Project

#### RHM 2401.6 B. Tech with Honours in Research Degree

For B. Tech with Honours in Research Degree, students need to engage in research internships and research projects, either from reputable research organizations like IIT, TIFR, etc. or in exceptional cases at FCRIT depending upon available infrastructure and domain expertize of the guide, in the similar technology discipline.

The proposed curriculum structure and examination scheme are available in the following tables.

In the Research Project Coursework, students are required to participate in Orientation courses/MOOC courses pertinent to their research area or contemporary technological trends. Additionally, they must fulfill assignment-based activities as part of their coursework.

In Research Project-I, the student is tasked with conducting an in-depth literature review, defining the research problem statement, and developing the research methodology.

In Research Project II, the student is responsible for executing the research methodology, analyzing results, and deriving sound conclusions. In Research Project-III, the student is required to compile a comprehensive report and either submit a research paper to a reputable journal or pursue patent filing.

Course Type	Sem	Course Code	Course Name	Course Name		achir hemo ontao Iours	e ct	C	Credits	Assi	gned
					L	Р	Т	L	Р	Т	Total
RPC	V	RPC501#	Research Project Coursework		2	6		2	3		5
RP	VI	RPI602@	Research Project – I						5		5
RP	VII	RP701@	Research Project- II						5		5
RP	VIII	RP802	Research Project-III						3		3
			Тс	otal	2	6			18		18

#### Table RHM 2401.6.1: Curriculum Structure for Honours in Research Degree Program

# Coursework for research projects can begin during the semester break following the fourth semester, lasting for five weeks.

@ Research projects activities shall begin during semester break following fifth, sixth and seventh semesters, with each break lasting approximately six weeks.

NOTE: Those students opting for Honours in Research are required to carry out their internship in the eighth semester from FCRIT only.

Table RHM 2401.6.2: Examination Scheme for Honours in Research Degree Program

**Examination Scheme** 

Course Type	Sem	Cour se Cod	Course Name		In-Semester Assessment		Durat The	am. ion for eory Hrs)	Total
		е		Continuous Assessment	Mid Sem. Exam.	(ESE)	Mid Sem	End Sem	
RPC	V	RPC501	Research Project Coursework	50					50
RP	VI	RPI602	Research Project – I	50		50**			100
RP	VII	RP701	Research Project- II	50		50**			100
RP	VIII	RP802	Research Project-III	50					50
		Total		200		100			300

\*\*ESE will be in the form of an Open Seminar presented before the Research Assessment Committee (RAC), comprising both Internal and External supervisors, alongside two senior faculty members.

RHM 2401.6 Award of Degree Certificate by the University of Mumbai

If the student completes the Honours/Minor/Honours in Research program but fails in any of the regular courses, then he/she shall not get any degree certificate at that point of time. Degree certificates shall be awarded only after passing the regular degree program and the Honours/Minor/Honours in Research program.

The Honours/Minor/Honours in Research program should be completed in four semesters only (semesters V to VIII).

The following FCRIT regulations related to examinations do not apply to Honours/Minors/Honours in Research Degree Programs as these are applicable for the entire examination and overall results of semesters.

- i. RE2404.2
- ii. RE2404.3
- iii. RE2404.4
- iv. RE2404.5

The students successfully completing the Honours/Minor/Honours in Research program Degree shall be awarded the degree designated as: "B. Tech in.....(regular) Engineering with Honours/Minor in (specialization)"

Example 1: Students who successfully complete B. Tech in Mechanical Engineering with a specialization in Supply Chain will be awarded the degree of "B. Tech in Mechanical Engineering with Honours in Supply Chain."

Example 2: Students who successfully complete B. Tech in Electrical Engineering with a Minor in Supply Chain will receive the degree of "B. Tech in Electrical Engineering with Minor in Supply Chain."

Example 3: Students who successfully complete B. Tech in Electronics and Telecommunication Engineering with an Honours in Research will receive the degree of "B. Tech in Electronics and Telecommunication Engineering with Honours in Research."

7

# Honors Syllabi

# Honors in IoT and Embedded systems

Course Type	Course Code	Course Name	Credits
НМС	ECHMCIE501	SENSORS & IOT PROTOCOLS	3

		Examination	Scheme		
Dis	tribution of Marks	8	Evon Dur	nation (Ung)	
In-semester	Assessment	~	Exam Duration (Hrs.)		
Continuous Assessment	Mid-Semester Exam (MSE)	End Semester Exam (ESE)	MSE	ESE	Marks
20	30	50	1.5	2	100

# **Pre-requisite:**

- 1. ESC203- Basic Electronics Engineering
- 2. BSC102- Engineering Physics-I
- 3. BSC103-Engineering Chemistry-I

# **Program Outcomes addressed:**

- 1. PO1: Engineering knowledge
- 2. PO2: Problem analysis
- 3. PO4: Conduct investigations of complex problems
- 4. PO5: Modern tool Usage
- 5. PO8: Individual and team work
- 6. PO9: Communication

# **Course Objectives:**

- 1. To impart knowledge of the fundamentals of IoT.
- 2. To familiarize students with various types of sensors used to measure physical quantities.
- 3. To familiarize students with electronics used to interface sensors in IoT.
- 4. To introduce students to the current state of the art in sensor technology.
- 5. To learn and implement various networking and communication protocols.

Module	Details	Hrs
	Course Introduction	01
	In today's interconnected world, the integration of sensors and Internet of Things (IoT) protocols is transforming how we interact with technology and our environment. This course will provide a comprehensive understanding of the principles and applications of sensors in IoT systems. Sensors are critical components that enable the collection of real-time data from the physical world, allowing for intelligent decision- making and automation across various domains, including healthcare, agriculture, smart cities, and industrial automation. Students will	

	explore various types of sensors, their working principles, and their	
	applications in different scenarios.	
	Moreover, the course delves into IoT protocols, which are essential	
	for enabling seamless communication between devices, networks,	
	and cloud services. Understanding these protocols, such as MQTT,	
	CoAP, and HTTP, is crucial for developing scalable and efficient IoT	
	solutions. By examining the design and implementation of IoT	
	architectures, students will gain insights into data transmission,	
	security, and the challenges faced in real-world applications.	
01.	Introduction to IoT	06-08
	Learning Objective/s:	
	<i>To learn basic concepts and technologies related to Internet of things.</i>	
	Contents:	
	Introduction -Defining IoT, Characteristics of IoT, Physical design of	
	IoT, Logical design of IoT, Functional blocks of IoT, Sources of IoT,	
	Defining Specifications About - Purpose & requirements, process,	
	domain model, information model, service, Functional view,	
	Operational view, Device and Component Integration, Application	
	Development, Case Study on Home automation.	
	Self-Learning Topics: Understanding the Issues and Challenges of a More Connected World	
	Learning Outcomes:	
	A learner will be able to	
	LO 1.1: Apply fundamental engineering concepts to summarize the characteristics and functional blocks of IoT. (P.I 1.3.1)	
	LO 1.2: Apply concepts of communication engineering to review the given resources and interpret the different types of models and Views of IoT. (P.I 1.4.1, P.I 9.1.1)	
	LO 1.3: Extract desired understanding and conclusions from resources to conduct a case study on a selected application of IoT. (P.I 2.4.4, P.I 9.1.2)	
02.	Basic Sensors and its interfacing	08-10
	Learning Objective/s:	
	To identify the appropriate sensor for a particular application.	
	To identify the electronic circuitry needed for interfacing sensors to IoT boards.	
	Contents:	
	Sensor fundamentals- Need for sensors in IoT, sensor characteristics	
	(output level, frequency response, output impedance, directivity).	
	Principle of sensing (capacitance – magnetism – inductance –	
	resistance – piezoelectric – pyroelectric )	
	resistance – piezoeicente – pyrocicente /	

03.	Current Trends in Sensors and Technology         Learning Objective/s:         To provide students with a comprehensive understanding of smart sensor technologies, their design principles, and applications in diverse fields such as automotive, environmental monitoring, and home automation.	07-09
	LO 2.5: Identify and learn the usage of tools to perform signal conditioning and circuit interfacing in order to connect sensors to IoT. (P.I. 1.3.1, P.I. 4.1.3, P.I 4.3.1, P.I 5.1.1)	
	LO 2.4: Apply concepts of electronics and communication engineering to summarize sensor connections and related peripheral circuits. (P.I 1.4.1)	
	LO 2.3: Identify the necessary sensor and actuator for the given real-time application. (P.I. 2.1.2)	
	LO 2.2: Apply engineering concepts to elaborate on the types and working principle of actuators. (P.I 1.3.1)	
	A learner will be able to LO 2.1: Apply fundamental engineering concepts to summarize the characteristics and working principle of sensors. (P.I 1.3.1)	
	Learning Outcomes :	
	Sensor interfacing using simulation software	
	Optical sources and detectors, Sensors based on polymer optical fibers	
	Transfer function and modelling of sensors	
	Self-Learning Topics:	
	Actuators- Need of actuators, all types of actuators and their working. Identification of sensor and actuator for real-time application	
	Interface Electronic Circuits- Sensor Connections, Excitation Circuits, Analog to Digital Converters, Noise in Sensors and Circuits, Batteries for Low-Power Sensors, Signal Conditioners	
	Humidity, Moisture Chemical and Biological Sensors (Capacitive Humidity Sensors, Resistive Humidity Sensors, Optical Hygrometers, Soil Moisture MQ series, Chemical Sensor Characteristics),	
	Presence, force, Pressure (Potentiometric Sensors, Piezoresistive Sensors, Optoelectronic Pressure Sensors)	
	Types of sensors-Working, principle and characteristics. Microphone, Optical, radiation and Displacement sensors (Photosensors: Photodiode, phototransistor and photo resistor, Thermal infrared sensors, Capacitive and Inductive Displacement Sensor, Magnetic Field Sensor, LDRs)	

	Smart Sensors_ Introduction, Primary sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface.Sensor Technologies_ Introduction, Film Sensors, Thick Film	
	Sensors, Thin Film Sensors, Semiconductor IC Technology— Standard Methods, Microelectromechanical Systems (MEMS), Nano-sensors	
	Artificial Microsystems for Sensing Airflow, Temperature and Humidity by Combining MEMS and CMOS Technologies Sensor Applications: Onboard Automobile sensors, Home appliances sensors, Aerospace Sensors, Sensors for Environmental Monitoring	
	Self-Learning Topics:	
	Biosensors for biomedical applications	
	Learning Outcomes : A learner will be able to	
	LO 3.1: Apply fundamental engineering concepts to summarize the characteristics,	
	working principle of smart sensors used in various sensor technologies. (P.I 1.3.1)	
	LO 3.2: Apply concepts of electronics and communication engineering to summarize	
	signal conditioning of smart sensors. (P.I 1.4.1)	
	LO 3.3: Apply fundamental engineering concepts to summarize MEMs and CMOS technologies. (P.I 1.3.1)	
	LO 3.4: Identify appropriate smart sensors for specific applications.(P.I. 2.1.2)	
04.	Networking protocols	05-06
	Learning Objective/s:	
	To teach the concept of the Internet of Things (IoT), including client-server and publisher models.	
	To educate students on IoT networking protocols and addressing methods used with IoT devices.	
	Contents:	
	OSI Model for the IoT, need of IoT protocols, TCP and UDP protocols at Transport layer, key features of transport layer protocols and security protocol at transport layer, Internet based Communication and IP protocols, IP addressing in IoT, Client-Server architecture.	
	<i>Self-Learning Topics:</i> <i>Survey on IoT protocols which use TCP and UDP ports at transport layer</i>	
	Learning Outcomes: A learner will be able to	
	LO 4.1: Comprehend the role of all the layer in OSI model of IoT architecture using basic engineering concepts. (PI: 1.3.1)	

	<ul> <li>LO 4.2: Apply the concepts of IoT and use appropriate tools to simulate the given network in groups. (PI: 1.4.1, P.I 5.1.2, P.I 8.3.1, P.I 8.2.4)</li> <li>LO 4.3: Extract desired understanding about the usage, benefits and limitations of the protocols at network layer and transport layer. (PI: 2.4.4)</li> </ul>				
05.	Communication protocols	07-09			
	<i>Learning Objective/s:</i> <i>Educate students with different communication protocols and their important features.</i> <i>Compare the different protocols used for communication purpose in IoT applications.</i>				
	Contents:				
	IoT Edge and IoT Cloud concept, application layer protocol: HTTP, M2M basics, architecture and M2M Gateway in IoT, Data link layer protocols : REST APIs, WebSocket, MQTT protocol, CoAP, LoRA, DDS, BLE, RFID, ZigBee, Wi-Fi.				
	Self-Learning Topics: Z-Wave, LoRAWAN and LWM2M				
	Learning Outcomes: A learner will be able to				
	LO 5.1 Apply concepts of electronics and communication engineering to summarize concepts of IoT Edge and Cloud architectures. (PI: 1.4.1)				
	LO 5.2: Compare the protocols at application layer and data link layer. (PI: 2.2.4) LO 5.3: Identify and select the appropriate wireless technology with justification for specific IoT networks. (PI: 2.2.4)				
06.	Message communication and data exchange formats				
	Learning Objective/s:				
	Teach students all the Message Communication protocols for connected devices, and Data exchange formats				
	To make students learn the different nodes of Node-RED for implementing the Communication Protocol				
	To make students justify the use of sensors and actuators and type of protocols required for various applications.				
	Contents:				
	Message Communication protocols for connected devices, Lightweight M2M Communication Protocols, Data exchange formats: JSON & XML, Node-Red concept, theory on use of GSM module and GPS module with IoT devices, case study on IoT applications such as smart city, medical and agriculture fields by selecting appropriate sensors, actuator and required protocols.				
	Self-Learning Topics: Flow control using NodeRed, learning the different nodes of Node-RED for implementing the Communication Protocol				
	Learning Outcomes: A learner will be able to LO 6.1: Elaborate on the lightweight M2M communication protocols using				

Total	45
Course Conclusion	01-02
LO 6.3: Read and understand the given resources to carry out case study in groups on specific use cases and present it recognizing each individuals contributions. (P.I 2.1.1,P.I. 8.3.1,P.I. 8.2.4, P.I. 9.1.2, P.I. 9.2.2)	
LO 6.2: Compare the various communication protocols, data exchange formats, addressing methods used in IoT applications. (PI: 2.2.4)	

### **Performance Indicators:**

<u>P.I. No.</u>	P.I. Statement
1.3.1	Apply fundamental engineering concepts to solve engineering problems.
1.4.1	Apply concepts of electronics and communication engineering and accepted practice areas to solve engineering problems.
2.1.1	Articulate problem statements and identify primary objectives and key constraints.
2.1.2	Identify engineering systems, variables, and parameters to solve the problems.
2.2.3	Identify existing processes/solution methods for solving the problem, including forming justified approximations and assumptions.
2.2.4	Compare and contrast alternative solutions to select the appropriate methodology.
2.4.4	Extract desired understanding and conclusions consistent with objectives and limitations of the analysis.
4.3.1	Use appropriate procedures, tools, and techniques to conduct experiments and collect data.
5.1.1	Identify modern hardware and software engineering tools, techniques and resources for engineering activities.
5.1.2	Use/adapt/modify/create tools and techniques to solve engineering problems.
8.2.4	Assess individual contributions to a team activity and provide feedback.
8.3.1	Present results as a team, with smooth integration of contributions from all individual efforts.
9.1.1	Read, understand and interpret technical and/or non-technical information.
9.1.2	Create clear, well-constructed, and well-supported written engineering documents and/or presentation.
9.2.2	Deliver effective oral presentations to technical or non- technical audiences.

Course Outcomes: A learner will be able to -

- 1. Comprehend on IoT architecture, models and Views, types of sensors, IoT Edge Nodes and Cloud Architecture (*LO 1.1, LO 1.2, LO 2.1,LO 2.2, LO 2.4,, LO 3.1, LO 3.2, LO 3.3, LO 4.1, LO 5.1, LO 6.1*)
- Analyse and identify the sensors, actuators and wireless technologies for a given application. (LO
   2.3, LO 3.4, LO 5.3)
- 3. Compare protocols at each layer of IoT architecture, data exchange formats and addressing methods. (*LO 4.3, LO 5.2, LO 6.2*)
- Perform simulations for sensor signal conditioning, circuit interfaces, IoT network configuration.
   (LO 2.5, 4.2)
- 5. Conduct case studies on given use cases and present it in groups. (LO 1.3, LO 6.3)

**CO-PO Mapping Table with Correlation Level** 

СОЮ	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
ECHEIE501.1	3											
ECHEIE501.2		3										
ECHEIE501.3		3										
ECHEIE501.4	3			3	3			3				
ECHEIE501.5		3						3	3			
Average												

**NOTE:** CO can be mapped to PO at level 3 if at least two PIs are associated with that CO; otherwise, it can be mapped at level 2.

#### **Text Books :**

- 1. Jacob Fraden, "Hand Book of Modern Sensors: physics, Designs and Applications", 2015, 3rd edition, Springer, New York.
- 2. Jon. S. Wilson, "Sensor Technology Hand Book", 2011, 1st edition, Elsevier, Netherland
- 3. D. Patranabis Sensor and Transducers (2e) Prentice Hall, New Delhi, 2003
- 4. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things, 2017.
- 5. Fundamentals of IoT Communication Technologies (Textbooks in Telecommunication Engineering), Springer Nature, ISBN-13 978-3030700829 ,2022.

# **Reference Books :**

- 1. Edited by Qusay F Hasan, Atta ur rehman Khan, Sajid A madani, "Internet of Things Challenges, Advances, and Application", CRC Press
- 2. John G Webster, Halit Eren, "Measurement, Instrumentation and sensor Handbook", 2014, 2nd edition, CRC Press, Taylor and Fransis Group, New York.
- 3. Nathan Ida, "Sensors, Actuators and their Interfaces: A Multidisciplinary Introduction", Second Edition, IET Control, Robotics and Sensors Series 127, 2020
- 4. Adrian McEwen, "Designing the Internet of Things", Wiley Publishers, 2013, ISBN: 978-1-118-43062-0
- 5. Dr.Raj Kamal,Internet of Things(IoT), Architecture and Design Principles.McGraw Hill Education.
- 6. Internet of things For Architects, Perry Lea Packt Publication, 2018

#### **Other Resources :**

- Vijay Madisetti and Arshdeep Bagha, "Internet of Things (A Hands-on-Approach)",1st Edition, VPT, 2019 1.

#### **IN-SEMESTER ASSESSMENT (50 MARKS)**

#### 1. Continuous Assessment (20 Marks)

Suggested breakup of distribution

Assignment on live problems/ case studies, wherein problems are given prior. Students are expected to research and collect required resources. They can use the resources and solve the problem on assigned date and time in Institute premises in presence of faculty member-10 marks

Software course projects-05 Marks

Regularity and active participation- 05 marks

# 2. Mid Sem Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

#### **END SEMESTER EXAMINATION (50 MARKS)**

End Semester Examination will be based on syllabus coverage up to the Mid Semester Examination (MSE) carrying 20% to 30% weightage, and the syllabus covered from MSE to ESE carrying 70% to 80% weightage.

Course Type	<b>Course Code</b>	Course Name	Credits
HMCIE	HMCIE602	EMBEDDED SYSTEM DESIGN WITH RTOS	03

Examination Scheme								
Distribution of Marks Exam Duration (Hrs.)								
In-semester	Assessment		Exam Du		Total			
Continuous Assessment	Mid-Semester Exam (MSE)	End Semester Exam (ESE)	MSE	ESE	Marks			
20	30	50	1.5	2	100			

#### **Pre-requisite :**

- 1. ESCLC103 Programming Laboratory I (C)
- 2. ESC203 Basic Electronics Engineering
- 3. HMCIE501 IoT Sensor Technologies

#### **Program Outcomes addressed :**

- 1. PO1: Engineering knowledge
- 2. PO2: Problem analysis
- 3. PO3: Design/Development of Solutions
- 4. PO5: Modern tool usage
- 5. PO11: Lifelong Learning

### **Course Objectives :**

- 1. Acquaint students with the fundamentals of embedded systems and various types of architectures.
- 2. Familiarize students with real-time operating systems (RTOS) and their application in embedded systems design.
- 3. Educate students to analyze real-time tasks, scheduling algorithms, and resource management in embedded systems.
- 4. Familiarize students with design methodologies for embedded systems, including hardware/software co-design.
- 5. Explore the implementation of embedded systems using RTOS platforms like FreeRTOS, VxWorks, and  $\mu$ C/OS.
- 6. Develop skills in debugging, performance optimization, and addressing real-time constraints in embedded systems.

Module	Details	Hrs
	Course Introduction:	01
	The Embedded System Design with RTOS (ESRTOS) course offers a fundamental understanding of an embedded systems, design aspects and real-time operating systems. It covers core topics like system architecture, selection of appropriate microcontrollers for embedded systems design and RTOS for embedded system applications. Course covers task scheduling, resource management in real-time environments, inter-task communication and embedded applications using RTOS on platforms such as ARM Cortex. The course aims to equip learners with the skills needed to design reliable embedded systems using RTOS. It emphasizes software	

	development, system design, and problem-solving. The course serves as		
	a prerequisite for learning advanced topics, including modern communication protocols and IoT-enabled embedded solutions.		
01.	Introduction to Embedded Systems	6	
	<i>Learning Objective/s:</i> To introduce learners to embedded system principles, architecture, and development processes for practical application in real-world design.		
	Contents:		
	<ul> <li>Introduction to Embedded Systems- Definition of Embedded System, difference between embedded systems and general purpose systems, characteristics, architectures, and classifications, major application areas.</li> <li>Core of Embedded Systems: Microprocessors, microcontrollers, DSPs (Digital Signal Processors), application specific ICs, Programmable logic devices, Commercial Off-The-Shelf Components (COTS), Chip on Board (COB), memory, sensors and actuators, communication interface, embedded firmware, reset circuit, oscillator and real time clock (RTC), watchdog timer (WDT), other system components. Embedded System Development Process: Specification, design, prototyping, and testing.</li> </ul>		
	Self-Learning Topics: Emerging trends in embedded systems and RTOS.		
	<i>Learning Outcomes :</i> A learner will be able to		
	LO1.1: Apply fundamental engineering concepts to solve numerical and		
	conceptual problems in embedded systems, including pull-up resistor		
	requirements, microcontroller constraints, and sensor specifications. (P.I. 1.3.1) LO1.2: Apply embedded system engineering concepts, including interrupts,		
	watchdog timers, memory management, and sensor-actuator integration, to solve		
	practical problems. (P.I. 1.4.1)		
	LO1.3: Analyze and decompose the embedded system development process		
	(specification, design, prototyping, and testing) into manageable sub-problems to address real-world design challenges. (P.I2.2.1)		
	LO1.4: Compare and select the most suitable target boards for given applications. (P.I2.2.4)		
02.	Embedded System Design	6	
	<i>Learning Objective/s:</i> <i>To familiarize learners with hardware/software co-design and system partitioning methods.</i>		
	Contents:		
	Design metric of embedded system, real time system's requirements, real time issues, interrupt latency. Design Methodologies: Hardware/software co-design, top-down and bottom-up design, system		
L		L	

	<ul> <li>partitioning to achieve a trade-off between system performance, flexibility, and cost.</li> <li>Introduction to ARM-v7-M (Cortex-M3), ARM-v7-R (CortexR4) and comparison in between them. Study of basic communication protocols like SPI, SCI (RS232, RS485), I2C, CAN, Field-bus (Profibus), USB (v2.0), Bluetooth, Zig-Bee. Embedded C-programming concepts for design examples.</li> <li>Embedded System Case Study: Analyze a real-world embedded system, focusing on design challenges such as hardware limitations, real-time system requirements, power management, and the corresponding design</li> </ul>	
	solutions implemented to address these issues.         Self-Learning Topics:         Case study of an advanced embedded application- Smart Home Security System, wearable health device-Continuouss glucose monitoring (CGM).	
	Learning Outcomes : A learner will be able to	
	LO2.1: Analyze the embedded system design problem by identifying key entities such as hardware components, software requirements, performance metrics, and constraints to address real-time system challenges. (PI: 2.1.2)	
	LO2.2: Compare and contrast different embedded system design methodologies to select the best approach for a given system. (PI: 2.2.4)	
	LO2.3: Design optimized embedded systems using system partitioning, co-design principles, and modern tools while creating clear and well-structured technical documentation. (PI: 3.2.4, 5.1.1, 5.2.2)	
	LO2.4: Implement real-time embedded systems with integrated communication protocols and power management, effectively conveying technical concepts through presentations and reports. (PI: 3.4.3, 5.1.1, 5.2.2)	
	Fundamentals of Real-Time Operating Systems (RTOS)	-
03.	<i>Learning Objective/s:</i> To introduce basic RTOS concepts, kernel architecture, and task scheduling.	8
	<b>Contents:</b> Introduction to RTOS: Definition of RTOS, types of RTOS, Major application Areas. RTOS Features: Understanding tasks, processes, threads, and context switching. Real-Time Scheduling: Preemptive verses non-preemptive, rate-monotonic scheduling (RMS), earliest deadline first (EDF). Inter-task Communication: Message queues, mailboxes, semaphores, and event-driven communication.	
	Self-Learning Topics: Explore different RTOS platforms like FreeRTOS, VxWorks, etc.	
	Learning Outcomes :	

~ ~ *	<i>Learning Objective/s:</i> <i>To apply RTOS in real-world embedded system design and performance optimization.</i>	-
05.	Embedded System Design with RTOS	(
	performance. (PI: 2.2.4)	
	versus dynamic allocation and heap management, to optimize system	
	LO4.4: Compare and evaluate memory management techniques, including static	
	2.1.2)	
	critical section conflicts in RTOS systems to propose effective solutions. (PI:	
	LO4.3: Analyze synchronization issues like deadlock, priority inversion, and	
	(PI: 1.4.1)	
	deletion, and priority adjustment, to solve practical embedded system problems.	
	LO4.2: Apply RTOS task management principles, including task creation,	
	based systems. (PI: 1.3.1)	
	and resource management to optimize timer and interrupt handling in RTOS-	
	LO4.1: Apply engineering concepts like real-time systems theory, control theory,	
	<i>Learning Outcomes :</i> A learner will be able to	
	Self-Learning Topics: Priority inversion problems in real-time systems.	
	<b>Contents:</b> RTOS Task Management: Task creation, deletion, and priority management. Task Synchronization and Coordination: Mutexes, critical sections, deadlock, priority inversion. Memory Management in RTOS: Static verses dynamic memory allocation, memory pools, heap management. Timers and Interrupt Handling: RTOS timer handling and interrupt service routines (ISR).	
	To explore task management, memory management, and synchronization in RTOS.	
04.	Learning Objective/s:	8
0.4	RTOS Programming	
	conflicts and message delays, for effective resolution and assessment. (PI: 2.2.1) LO3.4: Compare and select appropriate RTOS platforms and scheduling techniques for various embedded system applications. (PI: 2.2.4)	
	task communication, and divide them into interrelated sub-problems, like priority	
	LO3.3: Analyze real-time system challenges, such as task scheduling and inter-	
	synchronization, to manage system resources effectively and solve real-time system challenges. (PI: 1.4.1)	
	LO3.2: Apply RTOS concepts, including task creation, scheduling, and	
	(EDF), in embedded systems. (PI: 1.3.1)	
	algorithms, such as rate-monotonic scheduling (RMS) and earliest deadline first	
	LO3.1: Apply engineering fundamentals to optimize real-time scheduling	

[	RTOS for Embedded Systems: FreeRTOS, VxWorks, and µC/OS-II/III.	
	RTOS for Embedded Systems. FreekTOS, VXWorks, and µC/OS-II/III. RTOS Case Study: Design and development of an embedded system using an RTOS. Performance Considerations: Real-time constraints, CPU load balancing, power consumption. Debugging and Testing: Tools and techniques for debugging RTOS-based systems (JTAG, logic analyzers, oscilloscopes).	
	<i>Self-Learning Topics:</i> <i>Case studies of RTOS in automotive and industrial automation.</i>	
	<i>Learning Outcomes :</i> A learner will be able to	
	LO5.1: Design efficient embedded systems that meet real-time constraints using RTOS features such as task scheduling, resource management, and power optimization techniques. (PI: 3.2.4) LO5.2: Refine embedded system designs by incorporating debugging tools (e.g., JTAG, oscilloscopes) and performance analysis techniques, ensuring minimal latency and efficient resource utilization. (PI: 3.4.3) LO5.3:Utilize modern RTOS tools and platforms for task creation, synchronization, and system prototyping while integrating advanced debugging and testing techniques to optimize embedded system performance. (PI: 5.2.2, PI:11.2.2) LO5.4: Source and evaluate technical resources to explore advancements in RTOS-based embedded systems, ensuring continuous learning in debugging, testing, and real-time performance optimization. (PI: 5.1.1, PI: 11.3.1)	
06.	Advanced Topics in RTOS and Embedded Systems	6
	<i>Learning Objective/s:</i> <i>To explore advanced concepts like low-power design, embedded Linux, and IoT-driven applications.</i>	
	Contents:	
	Low-Power Embedded System Design: Energy-saving techniques, sleep modes, power management. Embedded Linux: Basics of Embedded Linux, boot loaders, kernel configuration, and root file systems. Security in Embedded Systems: Common security challenges and counter measures. Industry Trends: IoT, wearable computing, and autonomous systems using RTOS. Task creation and synchronization using FreeRTOS.	
	<i>Self-Learning Topics:</i> Explore current trends and applications of embedded Linux in IoT.	
	<i>Learning Outcomes :</i> A learner will be able to	
	LO6.1: Apply embedded system and RTOS concepts to provide secure, energy- efficient solutions involving task synchronization and power management. (PI: 1.3.1)	

# **Performance Indicators:**

#### <u>P.I.</u> No. <u>P.I. Statement</u>

- 1.3.1 Apply fundamental engineering concepts to solve engineering problem
- 1.4.1 Apply concepts of electronics and communication engineering and allied disciplines to solve engineering problems.
- 2.2.1 Reframe complex problems into interconnected sub-problems
- 2.1.2 Identify engineering systems, variables, and parameters to solve the problems
- 2.2.4 Compare and contrast alternative solutions to select the best methodology.
- 3.2.4 Apply formal idea generation tools to develop multiple engineering design solutions.
- 3.4.3 Refine a conceptual design into a detailed design within the existing constraints (of the resources)
- 5.1.1 Identify modern engineering tools such as computer-aided drafting, modeling and analysis; techniques and resources for engineering activities
- 5.2.2 Demonstrate proficiency in using discipline-specific tools.
- 11.2.2 Recognize the need and be able to clearly explain why it is vitally important to keep current regarding new developments in your field.
- 11.3.1 Source and comprehend technical literature and other credible sources of infromation

Course Outcomes: A learner will be able to -

- 1. Apply a foundational knowledge acquired in embedded system principles, architecture, to develop embedded system processes. (LO1.1, LO1.2, LO1.3, LO1.4)
- 2. Design embedded system using hardware/software co-design principles to optimize embedded system design. (LO2.1,LO2.2, LO2.3. LO2.4)
- Analyse core RTOS concepts, including task scheduling, kernel architecture, and intertask communication.(LO3.1, LO3.2, LO3.3, LO3.4)
- 4. Apply RTOS principles to manage task creation, synchronization, and memory management to optimize real-time performance.(LO4.1, LO4.2, LO4.3, LO4.4)
- 5. Design and optimize embedded systems using RTOS features, including real-time task management and performance analysis. (LO5.1, LO5.2, LO5.3, LO5.4)

6. Examine advanced concepts like low-power design, embedded Linux, IoT applications, and security challenges in RTOS-based systems. (LO6.1, LO6.2, LO6.3, LO6.4)

CO ID	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
HMCIE602.1	3	3									
HMCIE602.2		3	3		3						
HMCIE602.3	3	3									
HMCIE602.4	3	3									
HMCIE602.5			3		3						3
HMCIE602.6	3	3									
Average	3	3	3		3						3

# **CO-PO Mapping Table with Correlation Level**

# **Text Books :**

- 1. "Embedded Systems: Real-Time Operating Systems for ARM Cortex M Microcontrollers" by Jonathan W. Valvano, CreateSpace Independent Publishing, 3rd Edition (2020)
- 2. "Real-Time Embedded Systems: Design Principles and Practice" by Xiaocong Fan, Elsevier, 1st Edition (2020)
- 3. "Embedded Systems: Architecture, Programming and Design" by Raj Kamal, McGraw-Hill Education, 4th Edition (2020)
- 4. "Embedded System Design: A Unified Hardware/Software Introduction" by Frank Vahid, Pearson Publications, Hardcover – Import, 24 October 2001
- 5. "Programming Embedded Systems in C and C++" by Michael Barr and Anthony Massa, O'Reilly Media, 2nd Edition (2021)
- 6. "MicroC/OS-II: The Real-Time Kernel" by Jean J. Labrosse, Micrium Press, 3rd Edition (2012)
- 7. "Real-Time Systems: Design Principles for Distributed Embedded Applications" by Hermann Kopetz, Springer, 2nd Edition (2011)

# **Reference Books :**

- 1. "Real-Time Systems" by Jane W. S. Liu, Pearson, 2nd Edition (2000)
- 2. "The Art of Designing Embedded Systems" by Jack Ganssle, Newnes, 2nd Edition (2010)
- 3. "Embedded Linux Primer: A Practical Real-World Approach" by Christopher Hallinan, Prentice Hall, 2nd Edition (2010)
- 4. "Real-Time Systems: Theory and Practice" by David C. Liu, Elsevier, 2nd Edition (2021)
- 5. "Hands-On RTOS with Microcontrollers: Building Real-Time Applications" by Benjamin P. Grosser, Packt Publishing, 1st Edition (2022)
- 6. "Modern Embedded Computing: Designing Connected, Pervasive, Media-Rich Systems" by
- Raghunathan R. R., Morgan Kaufmann, 1st Edition (2021)
- "Embedded Systems: A Comprehensive Guide to Understanding Embedded Systems" by Mark G.
   E. Gallo, Independently Published, 1st Edition (2023)

# **Other Resources :**

NPTEL Course: Introduction to Real Time Embedded Systems Part I, by Prof. Rajib Mall, Prof.

- Amit Patra, and Prof. A. Routray, Computer Science and Engineering, IIT Kharagpur. Web link: <u>https://nptel.ac.in/courses/108105057</u>
- 2. NPTEL Course: Real Time Operating System, by Prof. Rajib Mall, Computer Science and Engineering, IIT Kharagpur. Web link: <u>https://onlinecourses.nptel.ac.in/noc20\_cs16/preview</u>
- Lab Workshop on Embedded RTOS, by Martin K M, Scientist 'F', and Rajesh M., Scientist 'D',
  3. NIELIT Calicut. Web link: <u>https://elearn.nptel.ac.in/shop/iit-workshops/completed/lab-workshop-on-embedded-rtos/?v=c86ee0d9d7ed</u>
- 4. NPTEL Course: Embedded Systems Design, by Prof. Anupam Basu, Computer Science and Engineering, IIT Kharagpur. Web link: <u>https://onlinecourses.nptel.ac.in/noc20\_cs14/preview</u>
- 5. NPTEL Course: Embedded Systems, by Prof. Santanu Chaudhary, Electrical Engineering, IIT Delhi. Web link: <u>https://nptel.ac.in/courses/108102045</u>

NPTEL Course: Embedded System Design with ARM, by Prof. Indranil Sengupta and Prof.

6. Kamalika Dutta, Computer Science and Engineering, IIT Kharagpur. Web link: https://archive.nptel.ac.in/courses/106/105/106105193/

# **IN-SEMESTER ASSESSMENT (50 MARKS)**

# 1. Continuous Assessment (20 Marks)

Suggested breakup of distribution

- a. Practical (Task based) Assignments (min 5 projects) 05 marks
- b. Class Test based on theory and practical assignments 05 marks
- c. Technical Report Writing (e.g., Project documentation, Video Transcript:) 05 marks
- d. Regularity and Active Participation 05 marks

# 2. Mid Semester Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

# END SEMESTER EXAMINATION (50 MARKS)

End Semester Examination will be based on syllabus coverage up to the Mid Semester Examination (MSE) carrying 20 to 30 % weightage, and the syllabus covered from MSE to ESE carrying 70 to 80% weightage.

# Honors in VLSI

Course Type	<b>Course Code</b>	Course Name	Credits
HMC	HMCVL501	CMOS VLSI	03

	E	xamination Sche	me		
Di	stribution of Marks	Exam Dura			
In-semester	Assessment	End Semester		Total	
Continuous Assessment	Mid-Semester Exam (MSE)	Examination (ESE)	MSE	ESE	Marks
20	30	50	1.5	2	100

### **Pre-requisite:**

- 1. BSC102 Engineering Physics-I
- 2. ECPCC304 Digital Circuit Design

#### **Program Outcome addressed:**

- 1. PO1: Engineering Knowledge
- 2. PO2: Problem analysis
- 3. PO3: Design/Development of Solution
- 4. PO5: Modern Tool Usage
- 5. PO8: Individual and Team work
- 6. P09: Communication
- 7. PO11: Lifelong Learning

# **Course Objectives:**

- 1. To learn the basic concepts of MOSFETs, layout, fabrication. and solve the problems to analyse the MOSFETs.
- 2. To introduce the basics of CMOS Inverter, NAND, NOR gate for different performance metrics.
- 3. To familiarise combinational and sequential circuits using different design styles.
- 4. To learn the working of RAM and ROM array.
- 5. To provide exposure on static timing analysis and CMOS testing.

Modul e	Details	Hrs.						
	Course Introduction	01						
	This course is personalized to provide a comprehensive essential principles and techniques involved in designing digital electronic circuits., which is foundational for modern electronic systems. As we delve into the details of fabrication process right from sand to silicon. We will gain valuable insights into the principles, methodologies, and tools that drive the creation of integrated circuits which is need of the hour.							
01.	<ul> <li>Crystal Growth, Wafer preparation and fabrication for VLSI Technology</li> <li>Learning Objective/s:         <ol> <li>To provide knowledge of IC fabrication processes and advanced IC technologies</li> <li>To introduce students with custom layout software tools</li> </ol> </li> <li>Semiconductor Manufacturing: Semiconductor technology trend, Clean rooms, Wafer cleaning and Gettering.</li> <li>Semiconductor Substrate: Crystal structure, Crystal defects, Czochralski growth, Float Zone growth, Bridgman growth of GaAs, Wafer Preparation and specifications</li> </ul>	12						

<ul> <li>editor.</li> <li>Self-Learning Topics: MOS Capacitances, Short Channel Effects</li> <li>Learning Outcomes: A learner will be able to         LO 1.1: Apply the fundamental concepts related to semiconductor and subs manufacturing processes. (P.I1.4.1)         LO 1.2: Analyze and compare different fabrication technological processes. ( 2.2.4)         LO 1.3: Design the stick diagram, followed by custom layout using layout edito a given Boolean equation. (P.I-5.1.2, P.I3.3.3)         LO 1.4: Identify existing methods for analyzing different process flow of fabrice for NMOS, PMOS and CMOS. (P.I2.1.3)         LO 1.5: Develop ability to refine a conceptual design into a detailed design thr simulations with any opensource back-end software (micro wind/m effectively. (P.I -1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.1.1, PI 8.2.1, PI 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)         O2. CMOS Inverters and its Analysis Learning Objective:         <ol> <li>To introduce MOS based inverters and circuit realization us different analysis. 2. To learn CMOS Inverter</li> <li>Analysis of CMOS Inverter:</li> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter. Dynamic Analysis of CMOS inverter Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverter Subjective Boolean function using equivalent CMOS inverter simultaneous switching.</li> </ol> </li> <li>Self-Learning Topics: Logical Effort Learning Topics: Logical Effort Learning Topics: Logical Effort Learning Topics: Logical Effort         Learning Outcomes: A learner will be able to         LO 2.1: Apply findamental engineering concepts to identify the operation of CIC</li> </ul>	
<ul> <li>A learner will be able to         <ul> <li>LO 1.1: Apply the fundamental concepts related to semiconductor and subsmanufacturing processes. (P.I1.4.1)</li> <li>LO 1.2: Analyze and compare different fabrication technological processes. (2.2.4)</li> <li>LO 1.3: Design the stick diagram, followed by custom layout using layout edito a given Boolean equation. (P.I-5.1.2, P.I3.3.3)</li> <li>LO 1.4: Identify existing methods for analyzing different process flow of fabrice for NMOS, PMOS and CMOS. (P.I2.1.3)</li> <li>LO 1.5: Develop ability to refine a conceptual design into a detailed design thrasimulations with any opensource back-end software (micro wind/ma effectively. (P.I-1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.1.1, PI 8.2.1, PI 9.1. 9.2.1, PI-11.2, PI-11.1.3)</li> </ul> </li> <li>O2. CMOS Inverters and its Analysis         <ul> <li>Learning Objective:</li> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuits</li> <li>Contents:</li> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inverter calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverter simultaneous switching.</li> </ul> </li> <li>Self-Learning Topics: Logical Effort         <ul> <li>Learner will be able to</li> <li>A learner will be able to</li> </ul> </li> </ul>	
<ul> <li>manufacturing processes. (P.I1.4.1)</li> <li>LO 1.2: Analyze and compare different fabrication technological processes. (2.2.4)</li> <li>LO 1.3: Design the stick diagram, followed by custom layout using layout edito a given Boolean equation. (P.I-5.1.2, P.I3.3.3)</li> <li>LO 1.4: Identify existing methods for analyzing different process flow of fabrica for NMOS, PMOS and CMOS. (P.I2.1.3)</li> <li>LO 1.5: Develop ability to refine a conceptual design into a detailed design thrasimulations with any opensource back-end software (micro wind/ma effectively. (P.I - 1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.2.1, PI 8.2.1, PI 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)</li> <li>CMOS Inverters and its Analysis         <ul> <li>Learning Objective:</li> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuit</li> <li>Contents:</li> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS inverter. Dynamic Analysis of CMOS inverte Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverter Support Calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> </ul> </li> <li>Self-Learning Topics: Logical Effort</li> <li>Learner will be able to</li> </ul>	
<ul> <li>2.2.4)</li> <li>LO 1.3: Design the stick diagram, followed by custom layout using layout edito a given Boolean equation. (P.I-5.1.2, P.I3.3.3)</li> <li>LO 1.4: Identify existing methods for analyzing different process flow of fabrica for NMOS, PMOS and CMOS. (P.I2.1.3)</li> <li>LO 1.5: Develop ability to refine a conceptual design into a detailed design three simulations with any opensource back-end software (micro wind/ma effectively. (P.I-1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.1.1, PI 8.2.1, PI 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)</li> <li>CMOS Inverters and its Analysis Learning Objective:         <ol> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuit Contents:                 <ul> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS inverter: Static Analysis of CMOS inve Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inve Calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> <li>Self-Learning Topics: Logical Effort</li> <li>Learner will be able to</li> </ul> </li> </ol></li></ul>	.I —
<ul> <li>a given Boolean equation. (P.I-5.1.2, P.I3.3.3)</li> <li>LO 1.4: Identify existing methods for analyzing different process flow of fabrica for NMOS, PMOS and CMOS. (P.I2.1.3)</li> <li>LO 1.5: Develop ability to refine a conceptual design into a detailed design thrasimulations with any opensource back-end software (micro wind/ma effectively. (P.I-1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.1.1, PI 8.2.1, PI. 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)</li> <li>O2. CMOS Inverters and its Analysis         <ul> <li>Learning Objective:</li> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuit</li> </ul> </li> <li>Contents:         <ul> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inver Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverter Calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> </ul> </li> <li>Self-Learning Topics: Logical Effort         <ul> <li>Learning Outcomes: A learner will be able to</li> </ul> </li> </ul>	
<ul> <li>for NMOS, PMOS and CMOS. (P.12.1.3)</li> <li>LO 1.5: Develop ability to refine a conceptual design into a detailed design thrasimulations with any opensource back-end software (micro wind/maeffectively. (P.1-1.3.1, P.13.4.1, P.1.5.1.1, PI 8.1.1, PI 8.2.1, PI 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)</li> <li>O2. CMOS Inverters and its Analysis         <ul> <li>Learning Objective:</li> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuits</li> </ul> </li> <li>Contents:         <ul> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inve Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverter calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> </ul> </li> <li>Self-Learning Topics: Logical Effort</li> <li>Learning Outcomes: A learner will be able to</li> </ul>	for
<ul> <li>simulations with any opensource back-end software (micro wind/ma effectively. (P.I -1.3.1, P.I3.4.1, P.I.5.1.1, PI 8.1.1, PI. 8.2.1, PI. 9.1. 9.2.1, PI-11.1.2, PI-11.1.3)</li> <li>O2. CMOS Inverters and its Analysis Learning Objective:         <ol> <li>To introduce MOS based inverters and circuit realization us different analysis.</li> <li>To learn CMOS Inverter, NAND, NOR and complex logic circuits</li> </ol> </li> <li>Contents:         <ol> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inve Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inve Calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> </ol> </li> <li>Self-Learning Topics: Logical Effort</li> <li>Learning Outcomes: A learner will be able to</li> </ul>	ion
Learning Objective:         1. To introduce MOS based inverters and circuit realization us different analysis.         2. To learn CMOS Inverter, NAND, NOR and complex logic circuits         Contents:         • Circuit Operation of CMOS Inverter         • Analysis of CMOS Inverter: Static Analysis of CMOS inve Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inve Calculation of rise time, fall time and propagation delay         • Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.         Self-Learning Topics: Logical Effort         Learner will be able to	gic)
<ul> <li>Circuit Operation of CMOS Inverter</li> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inverter Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverCalculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> <li>Self-Learning Topics: Logical Effort</li> <li>Learner will be able to</li> </ul>	-
<ul> <li>Analysis of CMOS Inverter: Static Analysis of CMOS inverted Calculation of all critical voltages and noise margins. Design symmetric CMOS inverter. Dynamic Analysis of CMOS inverted Calculation of rise time, fall time and propagation delay</li> <li>Logic Circuit Design: Analysis and design of 2-I/P NAND, NOR complex Boolean function using equivalent CMOS inverter simultaneous switching.</li> <li>Self-Learning Topics: Logical Effort</li> <li>Learner will be able to</li> </ul>	
Self-Learning Topics: Logical Effort         Learning Outcomes:         A learner will be able to	er.
A learner will be able to	of ter:
LO 2.1: Apply fundamental engineering concepts to identify the operation of Cl	of ter:
Inverter, NAND and NOR gate (P.I1.3.1)	of ter:
LO 2.2: Identify basic concepts of CMOS Inverter and analyze all the l performance metrics of VLSI design (Noise margin, Propagation delay, Po dissipation and Area.in static and dynamic state (P.I 2.1.3)	of ter: and for
LO 2.3: Identify the relevant data from the resources to design NAND and NOR in terms of CMOS Inverter to arrive to an optimal design. (P.I-3.3.3,)	of ter: and for VOS usic

	LO 2.4: Develop ability to learn to solve the critical voltages of CMOS Inverter and design it through Think-Pair-Solo and present effectively. (P.I-1.4.1, P.I-2.3.1, P.I-3.1.6, PI 8.1.1, PI 8.2.1, PI 9.1.1, PI 9.2.1, PI 11.1.2, PI. 11.1.3)						
03.	<ul> <li>MOS Circuit Design Styles: Learning Objective/s:</li> <li>1. To introduce significance of various design styles of static and dynamic logic circuits.</li> <li>2. To help students articulate research paper, choose appropriate software and design style to meet to the specifications.</li> </ul>	6					
	<ul> <li>Contents:</li> <li>Design Styles: Static CMOS, pass transistor logic, transmission gate, Pseudo NMOS, C<sup>2</sup>MOS, Dynamic, Domino, NORA and Zipper.</li> </ul>						
	Self-Learning Topics: Corner Stitching analysis.						
	Learning Outcomes: A learner will be able to						
	<ul> <li>LO 3.1: Apply fundamental engineering concepts to solve problems of Combinational design styles. (P.I-1.3.1).</li> <li>LO 3.2: Apply concepts of electronics engineering and digital systems to solve engineering problems on sequential design styles (P.I-1.4.1).</li> </ul>						
	<ul> <li>LO 3.3: Analyze the basic concepts of different design styles for combinational and sequential circuits leading to conclusions in terms of merits and limitations. (P.I-2.4.4)</li> <li>LO3.4: Identify the relevant data from the resources (design styles), analyze and design the circuit for a given expression using an open source software. (P.I3.3.3, P.I-5.2.2)</li> </ul>						
	LO 3.5: Identify suitable criteria for evaluation of alternate design solutions using different styles for applications of digital design such as full adder, Decoder etc. and give the limitations for the same based on performance metrics. (P.I-2.4.3).						
04.	Semiconductor Memories Learning Objective:	7					
	1. To analyze various volatile, non-volatile and advanced memories.						
	<ul> <li>Contents:</li> <li>SRAM: 6T SRAM, operation, design strategy, leakage currents, read/write circuits, sense amplifier.</li> <li>DRAM: 3T &amp; 1T DRAM, operation modes, leakage currents, refresh operation, physical design.</li> <li>ROM Array: NAND and NOR, PROM, Flash Memory</li> </ul>						
	Self-Learning Topics: Fowler Nordheim Tunneling						
	Learning Outcomes: A learner will be able to						
	LO 4.1: Apply core principles of engineering to classify semiconductor memories. (P.I-1.4.1)						
	LO 4.2: Apply fundamental engineering concepts to solve the problems of 6T SRAM memories. (P.I-1.3.1)						
	LO 4.3: Identify and design NAND/NOR based ROM array for a given matrix using open-source tool. (P.I-3.1.6, P.I- 5.1.2)						

	LO 4.4: Identify the mathematical approach that applies to NAND and NOR flash memory. (P.I-2.1.3)	
	LO 4.5: Extract the understanding objectives and limitations of 6T SRAM / 3T DRAM (P.I-2.4.4)	
	LO 4.6: Design 6T SRAM / 3T DRAM using layout editor for the given specification. (P.I-3.3.3, P.I-5.3.3)	
05.	Datapath Design	5
	Learning Objective/s:	
	1. To highlight the fundamental issues in data path design and system level design.	
	Contents:	
	<ul> <li>Adder: CLA adder, MODL, Manchester carry chain and high speed adders like carry skip, carry select and carry save.</li> <li>Multipliers and shifter: Array multiplier and barrel shifter</li> </ul>	
	Self-Learning Topics: Booth Multiplier	
	Learning Outcomes : A learner will be able to	
	LO 5.1: Apply fundamental engineering concepts to different adders. (P.I-1.3.1)	
	LO 5.2: Compare and contrast alternative solutions to select appropriate adder (P.I- 2.2.4)	
	LO 5.2: Apply the Verilog constructs to solve combinational as well as sequential circuits. $(P.I - 1.4.1)$	
	LO 5.3: Identify the need of fast adders and analysis of different high-speed adders that applies to a given problem. $(P.I - 2.1.3)$	
06.	VLSI Clocking and System Design:	7
	Learning Objective/s:	
	To familiarize the concept of Clocking, Clocking Styles, distribution and low power design for a system	
	Contents:	
	• Clocking: CMOS clocking styles, Clock generation, stabilization and distribution	
	<ul> <li>Low Power CMOS Circuits: Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling</li> <li>I/O pads and Power Distribution: ESD protection, input circuits,</li> </ul>	
	output circuits, simultaneous switching noise, power distribution scheme	
	• Interconnect: Interconnect delay model, interconnect scaling and crosstalk	
	Self-Learning Topics: Nil	
	Learning Outcomes: A learner will be able to	

	Total 45
Students will be familiar with the knowledge of VLSI Tec devices from basics to system level designs with clocking	0.
Course Conclusion	01
LO.6.4: Identify and apply the effects of crosstalk in hi (P.I1.3.1)	eed digital interconnects.
LO.6.3: Model the delay introduced by interconnects u (e.g., Elmore delay) with accuracy (P.I2.3.1)	appropriate delay models
LO. 6.2: Identify the major components of power dissipate static, short-circuit, and leakage) that applies to a given	, <u>-</u>
LO 6.1: Identify the need of Clocking, and analyze generation and distribution. $(P.I - 1.4.1)$	erent clocking styles for

# CO-PO Mapping Table with Correlation Level

COID	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
HMC1.1	3	3	3		3			3	3		3
HMC1.2	3	3	3		3			3	3		3
HMC1.3	3	3	3		3						
HMC1.4	3	3									
HMC1.5	3	3									
Average	3	3	3		3			3	3		3

# **Performance Indicators:**

P.I. No.	P.I. Statement
1.3.1	Apply fundamental engineering concepts to solve engineering problems.
1.4.1	Apply concepts of electronics and communication engineering and allied disciplines to solve engineering problems.
2.1.3	Identify the mathematical, engineering and other relevant knowledge that applies to a given problem.
2.2.4	Compare and contrast alternative solutions to select the best methodology.
2.4.4	Extract desired understanding and conclusions consistent with objectives and limitations of the analysis
3.1.6	Determine design objectives, functional requirements and arrive at specifications
3.3.3	Identify relevant data from the given resources and arrive at an optimal design solution for particular specifications.
3.4.1	Refine a conceptual design into a detailed design within the existing constraints (of the resources)
5.1.1	Identify modern hardware and software engineering tools, techniques and resources for engineering activities.
5.1.2	Use/adapt/modify/create tools and techniques to solve engineering problems
9.1.1	Read, understand and interpret technical and/or non-technical information.
9.2.2	Deliver effective oral/presentations to technical or non-technical audiences.
11.1.2	Identify deficiencies or gaps in knowledge and demonstrate an ability to source the gap to close the gap

11.1.3	Develop ability to learn independently through methods distinct from instructor								
	provided materials.								
11.3.1	Source and comprehend technical literature and other credible sources of information								

# **Course Outcomes:**

- 1. Demonstrate a clear understanding of various MOS fabrication processes, CMOS fabrication flow and layout. (*LO 1.1, LO 1.2, LO1.3, LO1.4, LO 1.5*)
- 2. Design and analyse CMOS based inverters, NAND and NOR Gate. (LO 2.1, LO2.2, LO 2.3, LO 2.4)
- 3. Design and analyse different combinational/sequential circuits and realizations using different styles. (*LO3.1, LO 3.2, LO 3.3*)
- 4. Design semiconductor memories, adders and multipliers. (LO4.1, LO4.2, LO 4.3, LO4.4, LO4.5, LO 4.6)
- 5. Identify the strength and limitations of different adders and analyse the different types of adders. (*LO 5.1, LO 5.2, LO 5.3*)
- 6. Identify, analyse and design optimal interconnect model with crosstalk issues in VLSI Circuits(*LO 6.1, LO 6.2, LO6.3, LO6.4*)

# **Text Books :**

- 1. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw Hill, 3rd Edition, 2012
- 2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson Education, 2nd Edition.
- 3. CMOS VLSI Design-A Circuits and Systems Perspective, Neil H.E Weste, David Harris, Ayan Banerjee, 3 rd Edn, Pearson, 2009

# **Reference Books :**

- 1. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", Wiley, 2nd Edition, 2013
- 2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, Student Edition, 2013.
- 3. Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Pearson Education, 3rd Edition.
- 4. Introduction to VLSI Design-Mead & Convey, BS Publications, 2010.

# **Other Resources :**

- 1. NPTEL Course: CMOS Digital VLSI Design y Dr. Sudeb Dasgupta, IIT Roorkee: -Web link- CMOS Digital VLSI Design - Course
- 2. NPTEL Course: VLSI Design Verification and Test, By Dr.Santosh Biswas, Prof. Jatindra Deka, IIT Guwahati. Web link- https://nptel.ac.in/courses/106103016

# **IN-SEMESTER ASSESSMENT (50 MARKS)**

# 1. Continuous Assessment - Theory-(20 Marks)

Numerical Assignment/s (min 20 problems): 05 marks Class test based on above numerical assignment:05 marks each Simulation on problem statement/Article reading & summarization/Activity based study: 05 Marks

# Regularity and active participation:05 Marks 2. Mid Semester Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

# END SEMESTER EXAMINATION (50 MARKS)

aEnd Semester Examination will be based on syllabus coverage up to the Mid Semester Examination(MSE) carrying 30% weightage, and the syllabus covered from MSE to ESE carrying 70% weightage.

Course Type	Course Code	Course Name	Credits
HMC	HMCVL602	SYSTEM ARCHITECTURE	03

Examination Scheme						
Distribution of Marks			Even Duration (Ung)			
In-semester	Assessment		- Exam Duration (Hrs.) Total		Total	
Continuous Assessment	Mid-Semester Exam (MSE)	End Semester Exam (ESE)	MSE	ESE	Marks	
20	30	50	1.5	2	100	

# **Pre-requisite :**

1. CMOS VLSI Design

# **Program Outcomes addressed:**

- 1. PO1: Engineering knowledge
- 2. PO2: Problem analysis
- 3. PO3: Design/Development of Solutions
- 4. PO5: Modern Tool Usage
- 5. PO7:Ethics
- 6. PO8: Individual and Teamwork
- 7. PO9: Communication

# **Course Objectives:**

- 1. To comprehend system building blocks and computer architectures.
- 2. To acquaint the programable logic devices and System on Chips
- 3. To identify modern tools, Model base design and performance matrices in Field Programmable Logic Gate Implementation.
- 4. To Comprehend the system memory architecture and its performance indicators.

Module	Details	Hrs
	Course Introduction	01
	The System Architecture is the pioneering course to impart theoretical as well as practical skills in the field of system architecture design. This course prepares them to exploit the benefits of programmable logic and microprocessors to build more capable and exciting electronic systems. The System Architecture is also the prerequisite for system ASIC designs as well SoC field.	
01.	System Architectures	4 - 6
	<i>Learning Objective/s:</i> To analyse the system build blocks i.e., computer architectures and design interface for external peripheral communication.	
	Contents:	

	System Building Blocks: Overview of Computer Architecture- Memory Architecture -Van Numan & Harvard, Curriculum Structure, Core- Architecture -Micro-coded & Hard-Wired Coded, features, data frames, applications and limitations of Communication Protocols i.e., SPI, I2C, eSPI, CAN with data frames.		
	Self-Learning Topics: IoT Communication Protocols and its performance evaluation Learning Outcomes: A learner will be able to		
	LO 1.1: Differentiate computer architectures on memory interface. (P.I2.4.4) LO 1.2: Identify the communication protocol for desired applications such as interconnection of ICs, automobile sector, peripheral devices. (P.I2.1.1) LO 1.3: State the data format of a communication protocols and describe each fields meeting the requirement of communication standards. (P.I3.1.4) LO 1.4: Elicit the performance evaluation of desired communication protocol in teams. (P.I3.1.2)(P.I7.1.1) (P.I. 8.1.1) (P.I. 8.3.1) (P.I. 9.1.2) (P.I. 9.2.2)		
02.	Programmable Logic Devices	8 - 10	
	Learning Objective/s:		
	To analyse the architectures of CPLD and FPGA and enlisting technical specifications for VLSI design.		
	Contents:		
	Architecture of CPLD-I/O blocks, Switch Matrix, Product term allocator Microcell, Architecture of FPGA -Configurable logic blocks, Input/output block, Programmable interconnect, Comparison of FPGA and CPLD		
	Self-Learning Topics:		
	Enlist the vendor of CPLD and FPGA		
	Learning Outcomes: A learner will be able to		
	LO 2.1: Differentiate CPLD and PFGA based on architecture. (P.I2.4.4) LO 2.2: Identify the architectural component of CPLD / FPGA with the its neat sketch of interconnected sub system or blocks (P.I2.2.1) LO 2.3: Elicit the technical information of CPLD/FPGAs used in VLSI industry. (P.I3.1.2)(P.I7.1.1) (P.I. 8.1.1) (P.I. 8.3.1) (P.I. 9.1.2) (P.I. 9.2.2)		
03.	LO 2.4: Recognize the need of PLD's used in electronics designs. (P.I3.1.1) FPGA Implementation	8 - 1(	
	<i>Learning Objective/s:</i> To Select the engineering tools to design and implement electronics circuits on FPGA.		
	Contents:		
	FPGA Backend Tools, FPGA Implementation flow, mapping place and route, FPGA Editor, Timing Analysis, Synthesis and Optimization Techniques, Linux environment and TCL scripting.		
	Self-Learning Topics: Open-source tools for FPGA design.		
	Learning Outcomes :		

	A learner will be able to			
	LO 3.1: Identify the tools, languages used in FPGA design flow. (P.I5.1.1) LO 3.2: Identify the strength and limitations of back end tools, scripts used to FPGA implementation. (P.I5.2.1) LO 3.3: Describe the FPGA Design flow, synthesis, optimization techniques. (P.I 3.3.1)			
	LO 3.4: Identify the timing constraints to evaluate the synthesized RTL design. (P.I. 3.2.2)			
04.	SoC for Adaptive Computing			
	<i>Learning Objective/s:</i> <i>To Build SoC for adaptive computing by using modern tools and high level languages.</i>			
	Contents:			
	Embedded System on Chip (SoC) and Use of VLSI Circuit Design Technology, IP Core, FPGA Core with Single or Multiple Processors architectural features of Zynq SoC ,Zynq MPSoC ,Zynq RFSoC ,Kria, PYNC design environments,Use of Python language and libraries , Jupyter notebooks			
	Self-Learning Topics: Architectural features of Alveo			
	<i>Learning Outcomes:</i> A learner will be able to			
	LO 4.1: Identify architectural features i.e., processing and programmable logic of FPGA core to design SoC.(P.I3.3.3)			
	LO 4.2: Elicit the architectural features FPGA with single /Multicore processor. (P.I3.1.2)			
	LO 4.3: Identify the tools, languages used in designing SoC for adaptive computing. (P.I5.1.1) LO 4.4: Identify the strength and limitations of python design environment used to design SoC.(P.I5.2.1)			
05.	Integration of non-HDL modules	6 -8		
	<i>Learning Objective/s:</i> <i>To integrate the non HDL models and generate its HDL code used to design and implementation of electronic circuits.</i>			
	Contents:			
	Integrating non-HDL modules – Use of Tool box, Primitives of FPGA, Model base design for HDL code generation- continuous time modeling, discrete time modeling. Generate the HDL code of arithmetic circuits, control systems designs using Simulink of maths work.			
	<i>Self-Learning Topics: Design Feedback control system using Simulink and generate its HDL file.</i>			
	<i>Learning Outcomes:</i> A learner will be able to			
	LO 5.1: Identify the tools and techniques to generate HDL code of model base designs. (P.I5.1.1) LO 5.2: Identify the strength and limitations of tools used to generate the HDL code time base models. (P.I5.2.1)			
	LO 5.3: Formulate the complex multiplier model for Simulink design flow and state the steps to generate the HDL code of the complex multiplier. (P.I2.3.1)			

Contents: Memory Hierarchy in Laptop/Desktop, Domain specific accelerator, memory wall bottleneck, Implications in for processor design – energy break down , overhead, Memory performance matrix, High Bandwidth memory , bottle neck in memory access and MAC operation Cycle., Data Reuse, Parallel Architectures.	1
	,
<i>Learning Objective/s:</i> To apply the engineering fundamentals in memory systems and analyse the bottle necks in memory access.	?

## **Performance Indicators:**

#### P.I. No. P.I. Statement

- 1.2.1 Apply laws of natural science to an engineering problem.
- 1.3.1 Apply fundamental engineering concepts to solve engineering problems.
- 2.1.1 Articulate problem statements and identify primary objectives and key constraints.
- 2.1.2 Identify engineering systems, variables, and parameters to solve the problems
- 2.1.2 Identify engineering systems, variables, and parameters to solve the problems
- 2.2.1 Breakdown complex problem into interconnected sub systems and analyse by proper assumptions/ justification from information and resources.
- 2.2.2 Identify/ assemble/integrate mathematical tools to information and resources
- 2.2.4 Compare and contrast alternative solutions to select the best methodology.
- 2.3.1 Combine scientific principles and engineering concepts to formulate model/s (mathematical or otherwise) of a system or process that is appropriate in terms of applicability and required accuracy.

- 2.4.1 Apply engineering mathematics and computations to solve mathematical models
- 2.4.2 Produce and validate results through skilful use of contemporary engineering techniques
- 2.4.3 Identify sources of error in the solution process, and limitations of the solution.
- 2.4.4 Extract desired understanding and conclusions consistent with objectives and limitations of the analysis
- 3.1.1 Recognize that need analysis is key to good problem definition.
- 3.1.2 Elicit and document, engineering requirements from stakeholders
- 3.1.4 Extract engineering requirements from relevant engineering Codes and Standards such as IEEE, BIS, ISO, etc.
- 3.2.2 Identify suitable criteria for evaluation of alternate design solutions
- 3.3.1 Apply formal decision-making tools to select optimal engineering design solutions for further development
- 3.3.3 Identify relevant data from the given resources and arrive at an optimal design solution for particular specifications.
- Identify modern hardware and software engineering tools, techniques and resources for engineering 5.1.1 activities.
- 5.2.1 Identify the strengths and limitations of tools for (i) acquiring information, (ii) modelling and simulating, (iii) monitoring system performance, and (iv) creating engineering designs.
- 7.1.1 Follow ethical practices to create a document.
- 8.1.1 Recognize a variety of working and learning preferences; appreciate the value of diversity on a team
- 8.3.1 Present results as a team, with smooth integration of contributions from all individual efforts
- 9.1.2 Create clear, well-constructed, and well-supported written engineering documents and/or presentation.
- 9.2.2 Deliver effective oral presentations to technical or non- technical audiences.

Course Outcomes: A learner will be able to -

- 1. Identify the component of computer architectures, communication protocols and apply the knowledge in system design. (*LO 1.1, LO 1.2, LO 1.3, LO 1.4*)
- 2. Identify the building blocks of Programmable Logic devices and apply the knowledge in VLSI designs. (*LO 2.1, LO 2.2, LO 2.3, LO 2.4*)
- 3 Apply the knowledge of computer based tools to design and implement the electronics circuits on FPGA.

( LO 3.1, LO 3.2, LO 3.3, LO 3.4)

- 4 Design SoC for adaptive Computing. LO 4.1, LO 4.2, LO 4.3, LO 4.4, LO 5.1, LO 5.2, LO 5.3, LO 5.4)
- 5 Analyse the bottleneck in memory access. (*LO 6.1, LO 6.2, LO 6.3, LO 6.4*)

## **CO-PO Mapping Table with Correlation Level**

COID	PO1	PO2	PO3	PO4	PO5	<b>PO6</b>	<b>PO7</b>	<b>PO8</b>	PO9	PO10	PO11
HMCVL602.1		3	3				2	3	3		
HMCVL602.2		3	3				2	3	3		
HMCVL602.3			3		3						
HMCVL602.4		3	3		3						
HMCVL602.5	3	3									
Average	3	3	3		3		2	3	3		

### **Text Books:**

1. Computer Organization , V. Carl Hamacher , Zvonko Vranesic , Safwat Zaky, McGraw Hill

#### **Reference Books :**

- 1. Embedded System, Raj Kamal, Fourth Edition, 2020, McGraw Hill
- 2. Computer Organization and Architecture Designing for performance, William Stallings, Prentice Hall.
- 3. A Verilog HDL Primer, J. Bhasker, Third Edition, 1997, Star Galaxy Press

#### **Other Resources :**

- 1. https://www.pynq.io/boards.html
- 2. https://www.tulembedded.com/FPGA/ProductsPYNQ-Z2.html
- 3. Data sheets of Xilinx, AMD FPGA

## **IN-SEMESTER ASSESSMENT (50 MARKS)**

## 1. Continuous Assessment (20 Marks)

Suggested breakup of distribution

Design assignment on model base designs or SoC designs :10 Marks Article reading & summarization/poster creation: 05 Marks Regularity and active participation:05 Marks

# 2. Mid Semester Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

## END SEMESTER EXAMINATION (50 MARKS)

End Semester Examination will be based on syllabus coverage up to the Mid Semester Examination (MSE) carrying 20% to 30 % weightage, and the syllabus covered from MSE to ESE carrying 70 to 80% weightage.

# Honors in Network Security

Course Type	<b>Course Code</b>	Course Name	Credits
НМС	HMCNS501	COMMUNICATION SYSTEM AND NETWORK	03

	Examination Scheme								
Di	stribution of Marks	E D							
In-semester	Assessment	End Semester	Exam Dura	Total					
Continuous Assessment	Mid-Semester Exam (MSE)	Examination (ESE)	MSE	ESE	Marks				
20	30	50	1.5	2	100				

#### Pre-requisite:

1. Nil

## **Program Outcomes addressed:**

- 1. PO 1: Engineering knowledge
- 2. PO 2 : Problem analysis
- 3. PO 3 : Design solutions
- 4. PO 4 : Interpretation and conclusion
- 5. PO 5 : Modern tool usage
- 6. PO11 : Lifelong learning

#### **Course Objectives:**

- To impart knowledge on formation of networks with computer devices and their types, OSI layered models, types of networks and types of addressing used with computer networks at each layer in TCP/IP architecture.
- 2. To encourage students in performing analysis of different networking scenarios and requirements, comparison on wireless and wired networks.
- 3. To enable comprehending skills in students to illustrate various processes, architectures, networking scenarios and security requirements.
- 4. To teach students IoT and related applications in order to judge their ability to design solution for various networking scenarios.
- 5. To demonstrate to the students, use of various open source software for network analysis, packet tracing and packet sniffing.

Module	Details	Hrs.
	Course Introduction	01
	The "Communication system and Networks" course is crucial for students in understanding the types of communication, networks and need of security. This course aims to enhance the knowledge on modern telecommunication networks such as computer network, IoT and wireless networks, the advancements and current applications. This course provides the basic terms and background insights on networks for learning of Network security vertical essential in both academic and industry environments. This course	

	introduces the communication system and networks and concludes with an introduction on why security in essential in communication network.						
01.	Introduction to communication system and network						
	<ol> <li>Learning Objective:</li> <li>Educate students on the communication system and various blocks.</li> <li>To deliver knowledge on analogy and digital communication systems</li> <li>To introduce students about on digitization and packetization, wired and wireless networks.</li> </ol>						
	Contents:	]					
	Introduction to various Wired and wireless Communication channels, Introduction to analog communication : block diagram, overview of analog to digital conversion.						
	Digital communication : block diagram, Source coding and channel coding concept , Need of digitizing data for network communication, Introduction to packetization and related channel requirements	05.0					
	Security requirements for today's communication networks and IoT networks.	05-(					
	Self-Learning Topics:						
	Case study : Requirement of security in Fiber optic networks and Mobile networks						
	<i>Learning Outcomes:</i> A learner will be able to						
	LO 1.1: Illustrate the analog and digital communication system using block						
	diagrams as well as source and channel coding concepts. (PI:1.4.1)(2.2.4)						
	LO 1.2: Comprehend on the security requirements for today's communication Networks.(PI: 1.3.1)(11.3.1)						
	LO 1.3: Differentiate between wired and wireless channels and compare the						
	communication networks such as fiber optic, mobile, and IoT. (PI: 2.4.4)						
02.	Computer Communication Network	07-0					
	<ol> <li>Learning Objective:         <ol> <li>To educate students on the concept of formation of networks, topologies and types.</li> <li>To teach students the OSI layered model and TCPIP model.</li> <li>To introduce students about the hardware devices used for computer networks at different layers.</li> <li>To deliver knowledge on layer-wise protocols used with communication</li> </ol> </li> </ol>						
	networks.						
	<b>Contents:</b> Introduction to computer networks, Network types: LAN, MAN, PAN, CAN, WAN, SDWAN, Network topologies tree, bus, ring, mesh						
	OSI reference model 7 layer, 4 layer TCP/IP model, Protocols: definition, introduction to layer wise protocols used with communication networks.						
	Layer wise network hardware devices (NIC, Repeaters, Hubs, Bridges, Switches, Routers, Gateway and their comparison)						

	Self-Learning Topics:	
	Application layer protocols used for browsing Internet	
	<i>Learning Outcomes:</i> A learner will be able to	
	LO 2.1: State the use of various hardware devices used at each layer used with computer networks, protocols used at each layer in the OSI model. (PI: 1.4.1)	
	LO 2.2: Differentiate between the types of networks, their topologies, the	
	OSI model and TCP/IP model. (PI: 1.3.1) (PI: 2.4.4)	
03.	Network addressing and port numbering	07-08
	<ol> <li>Learning Objective:         <ol> <li>To give insights on protocol port numbering used with computer devices and their identification for reliable delivery.</li> <li>To deliver knowledge on the essential network and transport layer protocols used with computer networks</li> <li>To demonstrate use of IP utility commands in order to troubleshoot networks and use of open source software for analysis of protocol</li> </ol> </li> </ol>	
	Contents:	
	Addressing used with wired networks: physical, logical, port addressing, socket addressing.	
	Concept of reliable and unreliable delivery using TCP and UDP protocols, well known port numbers.	
	ARP and RARP protocol, host configuration: static and dynamic IP addressing, private and reserved IP addresses, IPv4, IPv6, DHCP and ICMP.	
	Troubleshooting of network using IP utility commands. *** demonstration during class Introduction to packet tracer or sniffer using Open source software. *** demonstration during class	
	Self-Learning Topics:	
	Investigating the contents of IP packets to identify the IP addresses, port numbers and type of delivery mechanism using any packet sniffing/packet tracer open source software.	
	<i>Learning Outcomes:</i> A learner will be able to	
	LO 3.1: Apply the knowledge on the TCP handshake, DHCP transition process	
	and use of ICMP messages. (PI: 1.4.1)	
	LO 3.2: Compare the types of IP addresses, IP versions and host configurations.	
	(PI: 2.4.4)	
	LO 3.3: Select and justify the use of transport layer protocols and port numbers	
	based on the scenarios provided. (PI: 2.1.3)	
	LO 3.4: Analyze the captured IP packets contents using available Open- source software and make use of IP utility commands to troubleshoot computer	
	network. (PI: 4.3.1), (PI: 5.1.2) (PI: 4.3.3) (PI: 5.2.2)	
		1

	<ol> <li>Learning Objectives:</li> <li>To introduce students to the wireless networks and protocols, mobile networks, satellite networks and sensor networks.</li> <li>To educate students on Wireless communication, Attacks and security protocols.</li> </ol>	
	<b>Contents:</b> Wireless communication, Wireless Networking Protocols, 802.11ax (Wi-Fi 6), 802.11ac (Wi-Fi 5), 802.11n (Wi-Fi 4), Bluetooth	
	Proliferation of mobile, satellite links and microwave/ radio frequency communication devices/networks, Attacks on mobile/cell phones, Satellite Jamming and Denial of Service Attacks	
	Wireless Security and Mobile Device Security, Attacks and Security Measures in Wireless LAN, IEEE 802.11 Wireless LAN, IEEE 802.11i Wireless LAN Security	
	Self-Learning Topics:	
	Case study: Nokia broadband and network security and solutions	
	Learning Outcomes:	
	A learner will be able to	
	LO 4.1: Enlist the wireless standards, security measures for various wireless	
	networks and present the network security and solutions based on case	
	studies.(PI: 1.3.1) (PI: 2.1.3) (PI: 11.1.3) (PI: 11.2.1)	
	LO 4.2: State the various attacks on mobile networks, Satellite networks and radio	
	networks. (PI: 1.4.1)	
	LO 4.3: Compare the features of various wireless networks. (PI: 2.4.4)	
05.	Internet of Things and security	07-08
	<ol> <li>Learning Objective/s:</li> <li>To teach the concept of Internet of things and related Iota protocols.</li> <li>To educate students on use of use of public and private cloud for IoT implementation.</li> <li>To deliver knowledge to students on vulnerabilities in IoT, digital certificates and machine identity management system in IoT.</li> </ol>	
	Contents:	
	Introduction to Internet of Things (IoT), Things in IoT, use of public and private cloud.	
	Introduction to popular IoT protocols used with IoT networks – MQTT and M2M, Security protocols for IoT systems.	
	Radio Frequency Vulnerabilities in the Internet of Things, digital certificates and machine identity management system in IoT	
	Self-Learning Topics: Use of cisco packet software to build basic IoT network	
	Learning Outcomes : A learner will be able to	
	LO 5.1: Apply knowledge on popular IoT protocols and compare MQTT and	

	Total	45
	Course Conclusion	01
	LO6.3: Apply knowledge on the various segmentation processes in networking and identify the strategy employed for Optimal Security Architecture through case study. (PI : 11.3.1)(PI : 11.1.3)	
	LO 6.2 : Compare physical, logical, and micro-segmentation. (PI :2.4.4)	
	with examples. (PI: 1.4.1) (PI :2.2.4)	
	LO 6.1: Justify the requirement of VLANs, VPNs, virtual routing and forwarding	
	Learning Outcomes: A learner will be able to	
	Real-world case studies to identify the segmentation strategy employed for Optimal Security Architecture	_
	Self-Learning Topics:	
	Micro-segmentation: network overlays/encapsulation	_
	<ul><li>Physical segmentation: in-band, out-of-band, air-gapped</li><li>Logical segmentation: VLANs, VPNs, virtual routing and forwarding, virtual domain</li></ul>	
	Contents:	
	<ul> <li>Learning Objective/s:</li> <li>1. Teach the concept of segmentation</li> <li>2. To introduce different types of segmentation scenarios</li> <li>3. Compare and Evaluate Segmentation Techniques for Optimal Security Architecture</li> </ul>	
06.	Network Segmentation	05-06
	<ul> <li>M2M, machine identity management system in IoT w.r.t use cases.</li> <li>(PI: 2.2.4) (PI: 2.1.3)</li> <li>LO 5.2: Design solutions for given IoT related application through selection of suitable communication protocol, addressing, components and cloud using opensource packet tracer software (PI: 3.1.6)(PI: 5.2.2)</li> <li>LO 5.3: Identify the vulnerabilities in IoT, security protocols and digital Certificates based on the case study preparation. (PI: 11.1.3) (PI: 11.3.1)</li> </ul>	
	M2M, machine identity management system in IoT w.r.t use cases.	

#### **Performance Indicators:**

- 1.3.1 Apply fundamental engineering concepts to solve engineering problems.
- 1.4.1 Apply concepts of electronics and communication engineering and allied disciplines to solve engineering problems.
- 2.1.3 Identify the engineering and other relevant knowledge that applies to a given problem
- 2.2.4 Compare and contrast alternative solution processes to select the best process.
- 2.4.4 Extract desired understanding and conclusions consistent with objectives and limitations of the analysis
- 3.1.6 Determine design objectives, functional requirements and arrive at specifications
- 4.3.1 Use appropriate procedures, tools, and techniques to conduct experiments and collect data
- 4.3.3 Represent data to facilitate analysis and explanation of the data, and drawing of conclusions

- 5.1.2 Use tools and techniques to solve engineering problems
- 5.2.2 Demonstrate proficiency in using discipline-specific tools
- 11.1.3 Develop ability to learn independently through methods distinct from instructor provided materials
- 11.3.1 Identify sources and comprehend information from technical literature

Course Outcomes: A learner will be able to -

- Apply knowledge of communication systems and protocols to illustrate various wired wireless communication, digital communication and security requirements in networks. (LO 1.1, LO 1.2, LO 2.1, LO 4.2, LO 5.1, LO 6.1)
- 2. Compare and contrast on wired and wireless networks, their topologies, the OSI model, TCP/IP model and network segmentation processes. (*LO 1.3, LO 2.2, LO 3.2, LO 4.3, LO 6.2*)
- 3. Analyse IP packets through the networks and justify the use of transport layer protocols, network layer protocols and port numbers based on the scenarios provided. (*LO 3.1, LO 3.3*)
- 4. Troubleshoot networks and analyse captured packets using open source network simulation software and design solutions for the given IoT related application. (LO 3.4, LO 5.2)
- Identify the network vulnerabilities and possible solutions based on appropriate case studies and illustrate the network segmentation strategies. (*LO 4.1, LO 5.3, LO 6.3*)

COID	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
HMCNS501.1	3	3									
HMCNS501.2	3	3									
HMCNS501.3				3	3						
HMCNS501.4	3	3	2	3	3						2
HMCNS501.5	3										2
Average	3	3	2	3	3						2

## **CO-PO Mapping Table with Correlation Level**

## **Text Books :**

- 1. Alberto Leon Garcia, "Communication Networks", McGraw Hill Education, Second Edition
- 2. Communications and Networking Behrouz A. Forouzan, Fifth Edition TMH, 2020
- 3. Vijay Madisetti and Arshdeep Bagha, "Internet of Things (A Hands-on-Approach)",1st Edition
- 4. Vijay K.Garg "Wireless Communications and Networking", Morgan–Kaufmann series in Networking

## **Reference Books :**

- 1. Computer Networks -- Andrew S Tanenbaum, 5th Edition, Pearson Education, 2013.
- 2. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things.
- 3. Vijay K.Garg "Wireless Communications and Networking", Morgan–Kaufmann series in Networking-Elsevier.
- 4. Nichols and Lekkas, "Wireless Security Models, Threats, and Solutions," by, McGraw-Hill, 2002, ISBN 0071380388.

## **Other Resources :**

- 1. SWAYAM and NPTEL course on "Computer Networks and Internet Protocol"
  - By Prof. Soumya Kanti Ghosh, Prof. Sandip Chakraborty | IIT Kharagpur
- 2. UDEMY course on "Introduction to Computer Networks" ps:www.udemy.com/course/introduction-to-computer-networks/
- UDEMY course on "Network Security Fundamentals"
- www.udemy.com/course/network-security-n

## **IN-SEMESTER ASSESSMENT (50 MARKS)**

#### 1. Continuous Assessment - Theory-(20 Marks)

- a) Case studies, Assignment, simulations: 10 Marks
- b) Quizzes (04) : 05 Marks
- c) Regularity and active participation: 05 Marks

## 2. Mid Semester Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

## END SEMESTER EXAMINATION (50 MARKS)

End Semester Examination will be based on syllabus coverage up to the Mid Semester Examination (MSE) carrying 20%-30% weightage, and the syllabus covered from MSE to ESE carrying 70%-80% weightage.

Course Type	<b>Course Code</b>	Course Name	Credits
HMC	HMCNS602	NETWORK SECURITY FUNDAMENTALS	03

Examination Scheme							
Di	stribution of Marks	E D					
In-semester	Assessment	End Semester	Exam Dura	Total			
Continuous Assessment	Mid-Semester Exam (MSE)	Examination (ESE)	MSE	ESE	Marks		
20	30	50	1.5	2	100		

#### **Pre-requisite:**

1. Introduction to Communication Networks and Security

#### **Program Outcomes addressed:**

- 1. PO1: Engineering knowledge
- 2. PO2: Problem analysis
- 3. PO6 : Societal aspects, safety, legal framework
- 4. PO7: Ethics
- 5. PO9 : Written communication
- 6. PO11: Life-long learning

### **Course Objectives:**

- 1. To introduce security in networking related to computers.
- 2. To make students differentiate between all types of security protocols related to OSI model.
- 3. To make understand various passive and active security attacks and vulnerabilities
- 4. To build an understanding on firewalls and IDS systems
- 5. To introduce students to security assessment and management.

Module	Details						
	Course Introduction						
	The "Network Security Fundamentals" course is crucial for students in understanding the security aspects for computer devices and networks. This course aims to enhance the knowledge on security attacks on networks, possible threats and defence mechanisms. This course concludes gives in sights on intrusion detection and prevention in computer networks and security assessment and management.						
01.	<ul> <li>Overview of Network security</li> <li>Learning Objective: <ol> <li>To educate students on network security, network vulnerabilities and secure wired networks.</li> <li>To deliver knowledge on solutions to secure wired and wireless devices</li> <li>To make students aware of the importance and effectiveness of network security and ethical ways to mitigate vulnerabilities.</li> </ol> </li> </ul>	05-06					

	Contents:						
	Network Security: Overview, Goals of Network Security, importance of effective network security strategies, Network security for computer device and in organization framework						
	Potential network vulnerabilities, ARP spoofing, Preventing ARP Spoofing, MAC flooding, Port mirroring, promiscuous mode, port stealing.						
	Tapping into transmission media, solutions to secure Ethernet LANs, Wi-Fi network security devices : active, passive and preventive.						
	Self-Learning Topics:						
	Case study on major security attacks – Mirai and Chain Reaction						
	<i>Learning Outcomes:</i> A learner will be able to						
	LO 1.1: Enlist various network vulnerabilities and security strategies. (PI: 1.3.1)						
	LO 1.2: Identify the security aspects at individual and organizational						
	level, security attacks and effect on public economy.						
	(PI: 1.4.1)(6.1.2)						
	LO 1.3: Compare various network security devices used with networks. (PI: 2.2.4)						
	LO 1.4 : Analyze technical aspects of network security by critically evaluating						
	ethical concerns related to responsible use and data privacy. (PI: 7.1.2)						
02.	Wired and wireless Network security protocols	07-08					
	<ul> <li>Learning Objective:</li> <li>1. To teach students network security protocols such as IPSec and related headers.</li> <li>2. To deliver knowledge on Firewalls and its types.</li> <li>3. To introduce students to wireless security protocols</li> </ul>						
	4. To engage students in carrying out case studies in wireless security tools						
	4. To engage students in carrying out case studies in wireless security tools						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload,</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi ,</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.11i Wireless LAN Security</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.11i Wireless LAN Security</li> <li>Self-Learning Topics:</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.11i Wireless LAN Security</li> <li>Self-Learning Topics: A survey on Wireless security tools being used by today's organizations</li> <li>Learning Outcomes:</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.11i Wireless LAN Security</li> <li>Self-Learning Topics: A survey on Wireless security tools being used by today's organizations</li> <li>Learning Outcomes: A learner will be able to</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.11i Wireless LAN Security</li> <li>Self-Learning Topics: A survey on Wireless security tools being used by today's organizations</li> <li>Learning Outcomes: A learner will be able to LO 2.1: Compare packet filter with proxy firewall, WEP and WPA protocols for</li> </ul>						
	<ul> <li>4. To engage students in carrying out case studies in wireless security tools</li> <li>Contents:</li> <li>Network layer security protocol: IPSec in detail : Tunnel mode, Transport mode, Authentication Header, Encapsulating security payload, Combining security associations</li> <li>VPN Firewall : proxy firewall, implementation of Packet filter firewall, dual firewall for Demilitarized Zone</li> <li>Wireless security protocols : Wired Equivalent Privacy (WEP), Wi-Fi , Protected Access (WPA), WPA2, IEEE 802.111 Wireless LAN Security</li> <li>Self-Learning Topics: A survey on Wireless security tools being used by today's organizations</li> <li>Learning Outcomes: A learner will be able to</li> <li>LO 2.1: Compare packet filter with proxy firewall, WEP and WPA protocols for wireless security. (PI: 2.4.4)</li> </ul>						

	protection of sensitive data, compliance with legal regulations, measures to safeguard individuals and organizations in a digitally connected society. (PI: 2.2.4) (PI: 6.2.1)						
03.	Intrusion detection systems for networks						
	<ol> <li>Learning Objective:         <ol> <li>To educate students to different types of Intrusion detection systems as well as prevention systems.</li> <li>To deliver knowledge on IDS based analysis and various generated alarms.</li> <li>To introduce students to usage of Snort and command line options for IDS.</li> </ol> </li> </ol>						
	Contents:						
	History of Intrusion Detection, Terminologies of Detection System (IDS), Types of Detection System – Network, Host and Distributed						
	Signature analysis, detecting traffic signatures, Identifying suspicious events, policy based, reputation based and anomaly based alarms, Intrusion Detection Vs Intrusion Prevention, IDS and IPS Architecture						
	Introduction to Snort and Command Line Options						
	Self-Learning Topics:						
	Snort Installation Scenarios						
	Learning Outcomes: A learner will be able to						
	LO 3.1: Compare host-based and network-based IDS systems, analysis and alarm						
	generation in ID system. (PI: 2.2.4)						
	LO 3.2: Identify and justify the appropriate type of Intrusion Detection System (IDS) and alarm generation mechanisms based on given scenarios,						
	(IDS) and alarm generation mechanisms based on given scenarios, considering societal needs such as data privacy and public safety.						
	( <i>PI: 2.4.4</i> ) ( <i>PI: 6.4.2</i> )						
	LO 3.3: Install Snort and use command line option for use in IDS. (PI: 11.1.3)						
04.	Application layer security for networks						
	<ul> <li>Learning Objectives:</li> <li>1. To educate students on different application layer protocols related to security</li> <li>2. To deliver knowledge on DNS and DHCP and their security features.</li> <li>3. To introduce students to emailing security, PGP scenario and, SNMP, SMLP</li> </ul>						
	Contents: E-Mail Security: Pretty Good Privacy protocol, S/MIME						
	Domain name system, Domain Name System Security Extensions, (DNSSEC) , DHCP spoofing attack, DHCP Snooping						
	Protocols and Ports in Windows Defender, Simple Network Management Protocol (SNMP): A Security Perspective						
	Self-Learning Topics:						

	A learner will be able to							
	LO 4.1: Illustrate the use of DHCP and DNS protocols and the associated							
	application layer security . (PI: 1.4.1)							
	LO 4.2: Justify the use of spoofing, snooping and SNMP to identify security vulnerabilities. (PI: 2.2.4)							
	LO 4.3: Compare PGP scenarios and S/MIME scenarios. (PI: 2.2.4)							
	LO 4.4: Enlist the benefits of Syslog Message Logging protocol and public safety services which rely on SNMP through case study report. (PI: 11.1.3) (PI: 9.1.2)							
05.	Transport layer security for networks							
	<ul> <li>Learning Objective/s:</li> <li>1. To make students understand the importance of transport layer security.</li> <li>2. To make students compare the TLS and SSL versions and HTTPs with normal browsing scenario.</li> <li>3. To teach students SSL protocol, sub-processes and SSH services</li> </ul>							
	Contents:							
	Transport-level Security: Web security considerations, benefits and limitations of transport layer security.							
	Secure Socket Layer and Transport Layer Security(TLS), SSL : Architecture, SSL Handshake Protocol, Change Cipher-Spec Protocol, Alert and Record protocol, Establishment of SSL Session, Secure Browsing – HTTPS, Secure Shell (SSH) services.							
	Self-Learning Topics:							
	HTTP vs HTTPs and TELENT vs SSH							
	Learning Outcomes :							
	A learner will be able to							
	LO 5.1: Illustrate the SSL protocol and process involved in securing data at							
	transport layer. (PI : 1.4.1)							
	LO 5.2: Analyse the use of HTTPS and SSH in contributing to a safer and more trustworthy digital society. PI: (2.2.4) (PI: 6.4.2)							
	LO 5.3: Justify the use of transport layer security and its benefits in protecting							
	<i>user privacy and ensuring data integrity in digital transactions. (PI :2.4.4)</i>							
06.	Security Assessment	05-06						
	<ul> <li>Learning Objective/s:</li> <li>1. To develop ability of reading technical reports on security assessment.</li> <li>2. To make students identify key performance and risk indicators in terms of security assessment</li> </ul>							
	Contents:							
	Technical and administrative data collection and processing, Account management, Management review and approval Key performance and risk indicators, Backup verification data							
	Training and awareness, Disaster Recovery (DR) and Business Continuity (BC)							
	Self-Learning Topics:							

Total	45
Course Conclusion	01
LO6.3 : Learn and interpret the security assessment reports. (PI: 11.1.3)PI: (11.3.1)	
LO 6.2: Comprehend on Training and awareness and Disaster Recovery. PI: (1.4.1)	
LO 6.1: List key performance and risk indicators in terms of security assessment . PI: (1.3.1)	
Learning Outcomes: A learner will be able to	
Real-world examples to demonstrate the value of comprehensive data collection in security management.	
Peal world argumples to demonstrate the value of comprehensive data collection in	ı.

#### **Performance Indicators:**

P.I. No.	P.I. Statement
1.3.1	Apply fundamental engineering concepts to solve engineering problems.
1.4.1	Apply concepts of electronics and communication engineering and allied disciplines to solve engineering problems.
2.2.4	Compare and contrast alternative solution processes to select the best process.
2.4.4	Extract desired understanding and conclusions consistent with objectives and limitations of the analysis
6.2.1	Comprehend legal requirements relevant to engineering design and propose solution complying to engineering standards.
6.4.2	Apply principles of preventive engineering and sustainable development to an engineering activity or product relevant to the discipline.
7.1.2	Recognize and articulate the issues involved in ethical case studies.
9.1.2	Produce clear, well-constructed, and well- supported written engineering documents
11.1.3	Develop ability to learn independently through methods distinct from instructor provided materials
11.3.1	Source and comprehend technical literature and other credible sources of information

Course Outcomes: A learner will be able to -

- 1. Apply fundamental engineering and communication concepts to comprehend the knowledge on various network vulnerabilities, security aspects, social responsibilities, ethical concerns. (*LO 1.1, LO 1.2, LO 1.4, LO 4.2, LO 5.2, LO 6.1*)
- 2. Identify the types of firewalls, IDS, network vulnerabilities and use of security protocols at the different layers in the TCP/IP model for the given networking scenarios. (*LO 2.2, LO 2.3, LO 3.2*),
- 3. Compare and contrast on various network security devices, firewalls, intrusion detection systems and related alarms to relate their use for a given application. (*LO 1.3, LO 2.1, LO 3.1, LO 4.3, LO 5.3*),
- 4. Justify the use of transport layer and application layer security protocols such as SSL, SSH, DHCP, DNS, PGP, S/MIME, SNMP for real world scenarios. (*LO 4.1, LO 5.1, LO 6.2*)
- 5. Identify network security issues, required security protocols, management and assessment reports through appropriate case studies. (*LO 4.4, LO 6.3*)

## **CO-PO Mapping Table with Correlation Level**

COID	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
HMCNS602.1	3	3				3	2				
HMCNS602.2	3	3				3					
HMCNS602.3	3	3									
HMCNS602.4	3										
HMCNS602.5									2		3
Average	3	3				3	2		2		3

#### **Text Books :**

- 1. TCP/IP protocol suite Behrouz A. Forouzan, Fifth Edition TMH, 2013.
- 2. Internet Security: A Hands-on Approach, by Wenliang Du, Third edition, 2022
- 3. Understanding communications and Networks, 3rd Edition, W.A.Shay, Cengage Learning
- 4. Nichols and Lekkas, "Wireless Security Models, Threats, and Solutions," by, McGraw-Hill, 2002, ISBN 0071380388.
- 5. Network Security: Private Communication In A Public World, 2nd Edn, by Charlie Kaufman, Radia Perlman, 2016

### **Reference Books :**

- 1. An Engineering Approach to Computer Networks-S.Keshav, 2nd Edition, Pearson Education, 2015.
- 2. Data and Computer Communications, William Stallings, 10th Edition, Pearson Education, 2014.
- 3. Vijay K.Garg "Wireless Communications and Networking" ,Morgan-Kaufmann series in Networking-Elsevier
- Cryptography and Network Security Principles and Practice | Seventh Edition
   | By Pearson by Stallings William, 2017

#### **Other Resources :**

1. Reports of security assessment of various organisation : recent ones will be provided from websites

#### **IN-SEMESTER ASSESSMENT (50 MARKS)**

#### 1. Continuous Assessment - Theory-(20 Marks)

- a) Case studies and Assignments related to this course : 10 Marks
- b) Quizzes (04): 05 Marks
- c) Regularity and active participation: 05 Marks

#### Mid Semester Exam (30 Marks)

Mid semester examination will be based on 40% to 50% syllabus.

## END SEMESTER EXAMINATION (50 MARKS)

End Semester Examination will be based on syllabus coverage up to the Mid Semester Examination (MSE) carrying 20%-30% weightage, and the syllabus covered from MSE to ESE carrying 70%-80% weightage.